模拟集成电路符号化低阶模型自动生成方法与应用

Automatic Generation Method of Low-order Models for Analog Integrated Circuits with Applications

胡翰彬 微纳电子学系
导师：施国勇 教授

Hanbin Hu, Dept. of Micro/Nano-electronics
Advisor: Prof. Guoyong Shi

Master Degree Defense, Shanghai Jiao Tong University, January 14, 2016

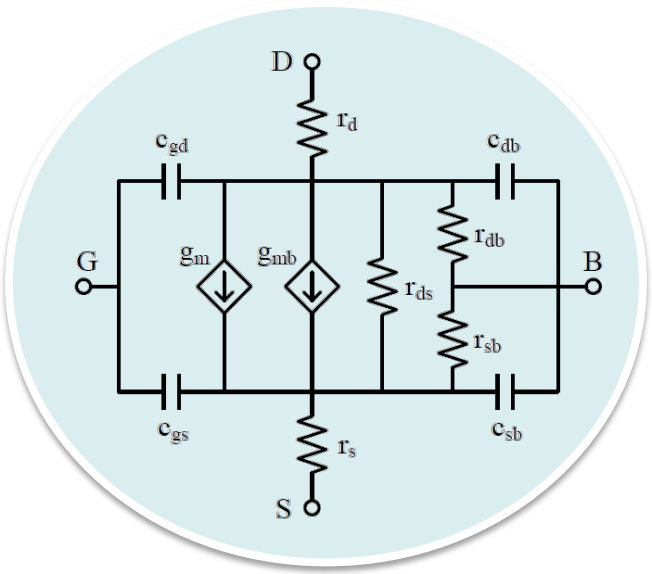
Outline

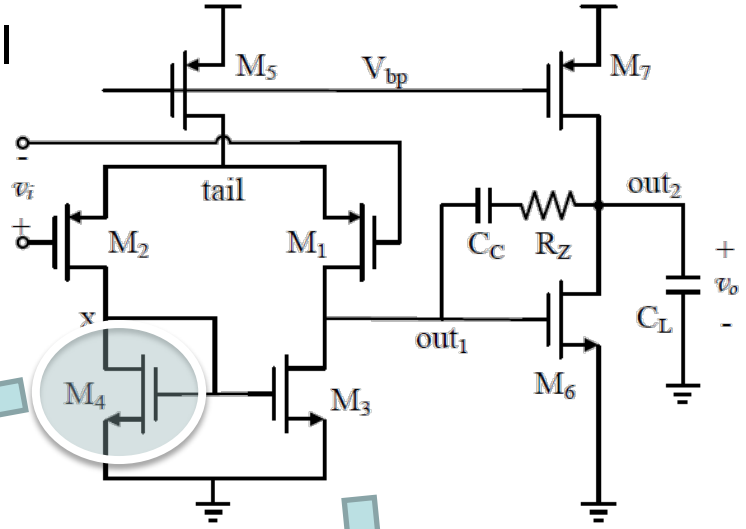
- Research motivation
- Background review
- **Main contribution**
  - Topology simplification algorithm
  - Applications (Time-domain & CMRR/PSRR)
- Experimental results
- Conclusion

Motivation for Model Order Reduction

- State of Art in Analog Circuit Design

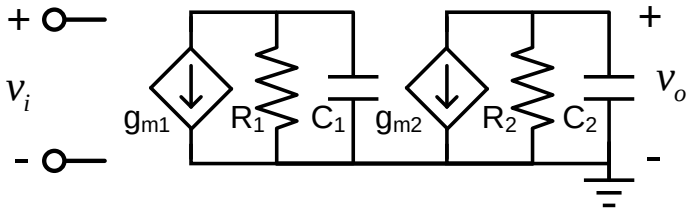
High-order model





How to generate?

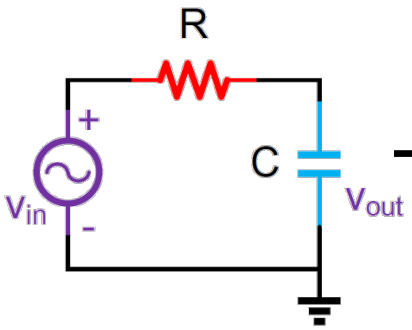
Low-order model



- Hard to capture principal elements in analog circuits

Symbolic Analysis

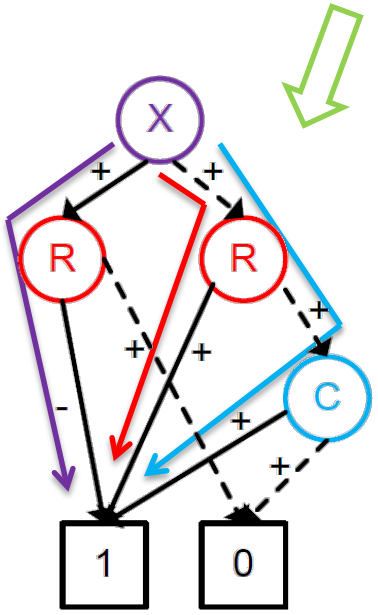
- Graph-Pair Decision Diagram – A BDD-Based Structure
- A topology-based analysis method



$$H(s) = \frac{1}{X} = \frac{G}{G + sC} \longrightarrow -XG + G + sC = 0$$

Construct

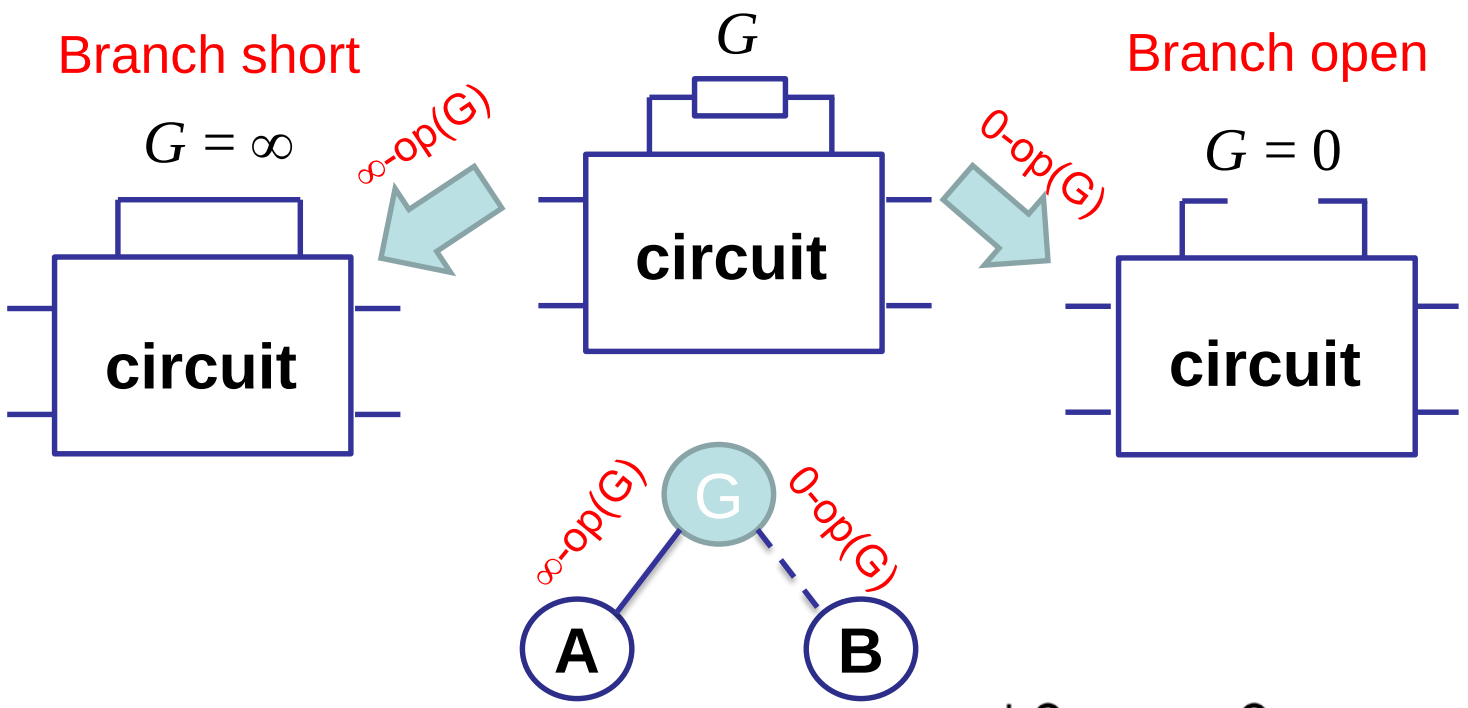
This diagram actually encodes the circuit topology



1-paths in the GPDD are symbolic terms

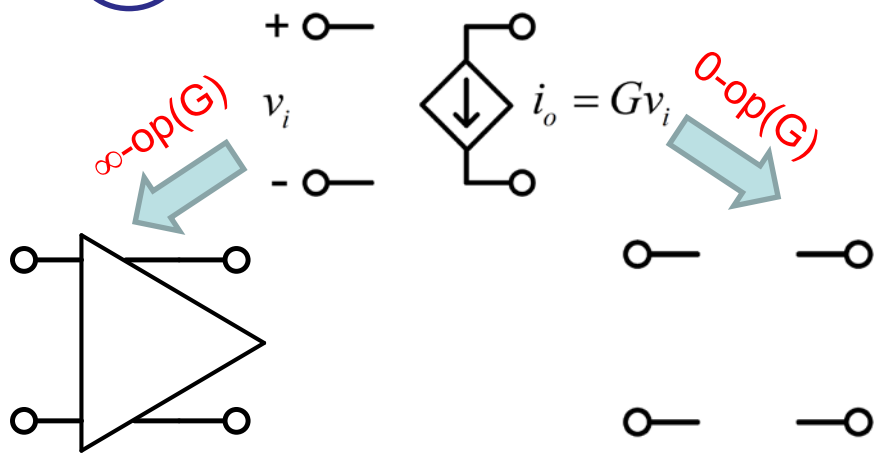
G. Shi (TCAD, 2013)

Two Operations for Topology Reduction in GPDD



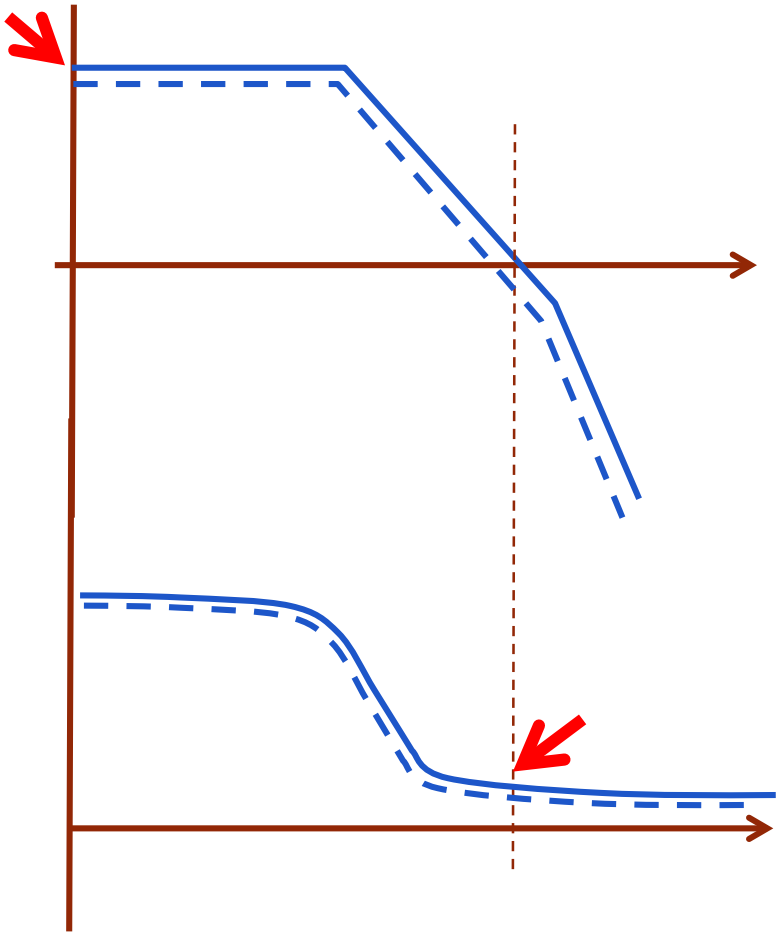
Admissible elements:
VCVS / CCCS / VCCS / CCVS

R / L / C



Significance Definition

- Significance from two operations



Fitness at ∞-op

$$F_{\infty-op} = \sqrt{\text{Rel. Gain Err.}^2_{\infty-op} + \text{Rel. PM Err.}^2_{\infty-op}}$$

⇩

Significance: $S = \min\left\{F_{\infty-op}, F_{0-op}\right\}$

⇧

Fitness at 0-op

$$F_{0-op} = \sqrt{\text{Rel. Gain Err.}^2_{0-op} + \text{Rel. PM Err.}^2_{0-op}}$$

Low-order Model Procedure

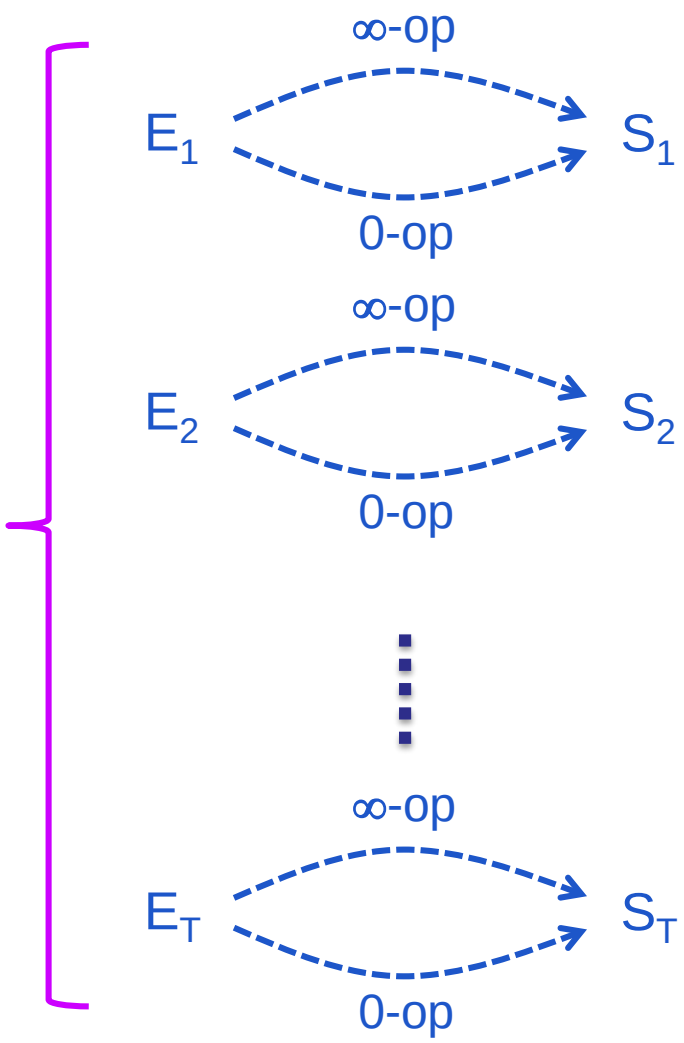
Bias the circuit to get nominal AC values (HSPICE)

Preprocess (Delete unnecessary circuits)

for each symbol do {
    significance evaluation
} (GPDD)

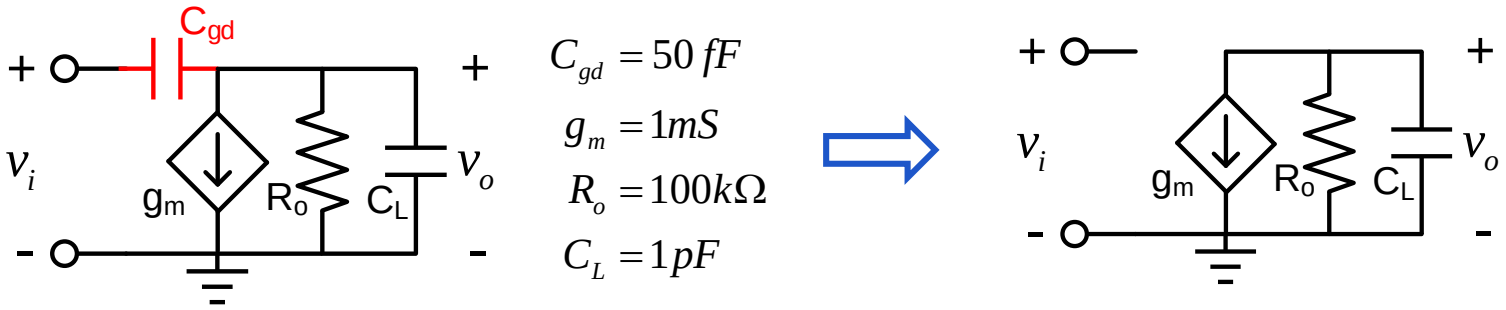
Sort symbols by significance

Eliminate
N least significant symbols
(N by trial-and-error)



Example

- Significance calculation

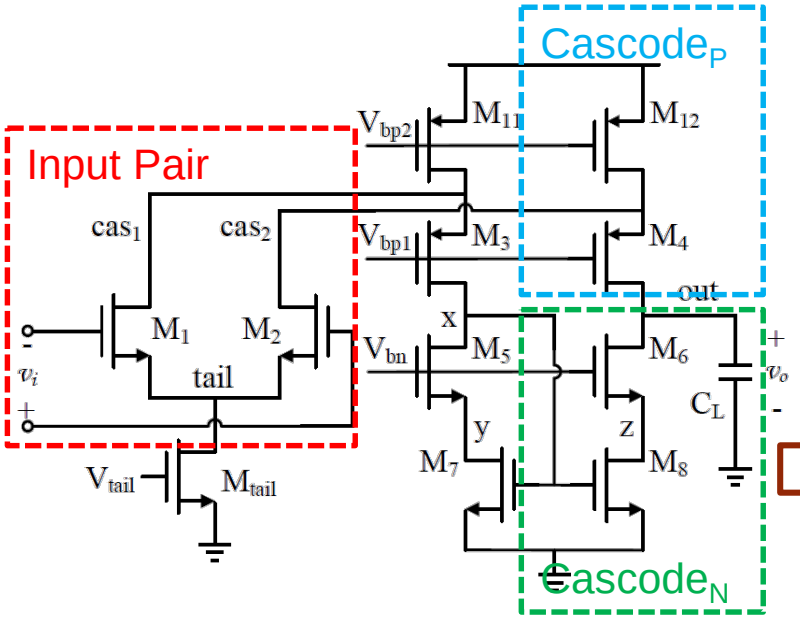


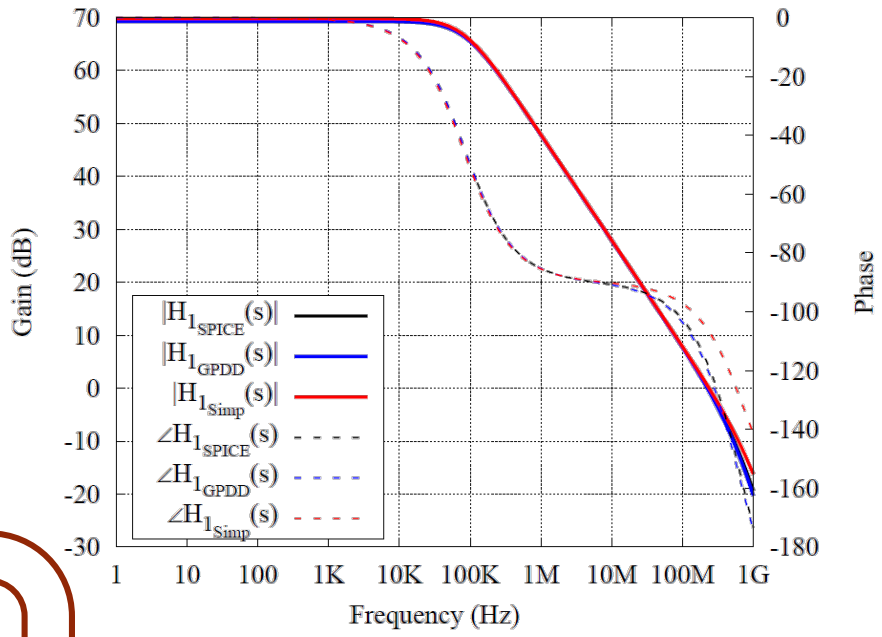
Symbol	Operation	ε	$\varepsilon_{\infty\text{-op}}$	$\varepsilon_{0\text{-op}}$
C_{gd}	0-op	3.28e-02	1.41e+00	3.28e-02
C_L	0-op	1.23e-01	Inf / NaN	1.23e-01
R_o	0-op	3.09e+00	Inf / NaN	3.09e+00
g_m	0-op	4.85e+00	Inf / NaN	4.85e+00

- Process abnormal value

Test Circuit 1

- Folded-cascode opamp



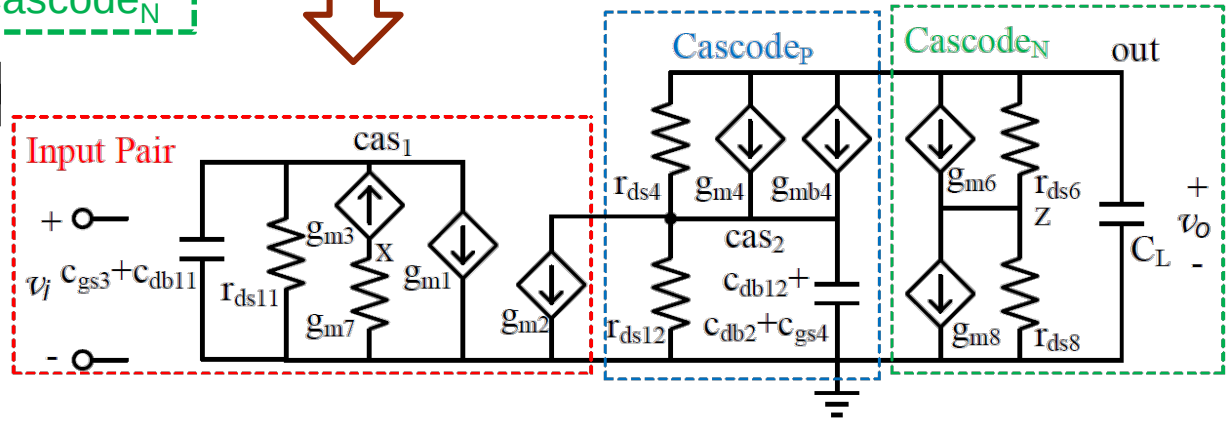


$$A_v = G_m R_o = -g_{m1}\left[\left(R_{out,4}\right) \| \left(R_{out,6}\right)\right]$$

$$R_{out,4} = \left[g_{m4}\left(r_{ds2} \| r_{ds12}\right)\right] r_{ds4}$$

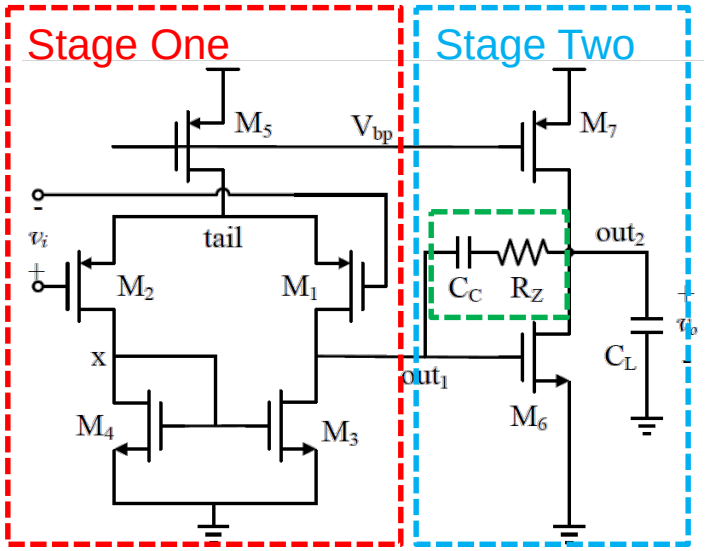
$$R_{out,6} = \left(g_{m6} r_{ds8}\right) r_{ds6}$$

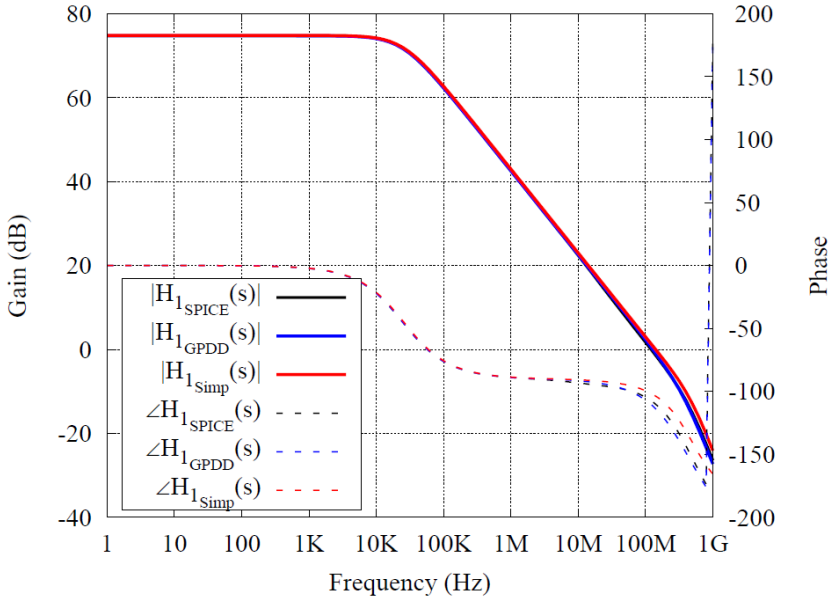
Matches textbook result!



Test Circuit 2

Two-stage opamp

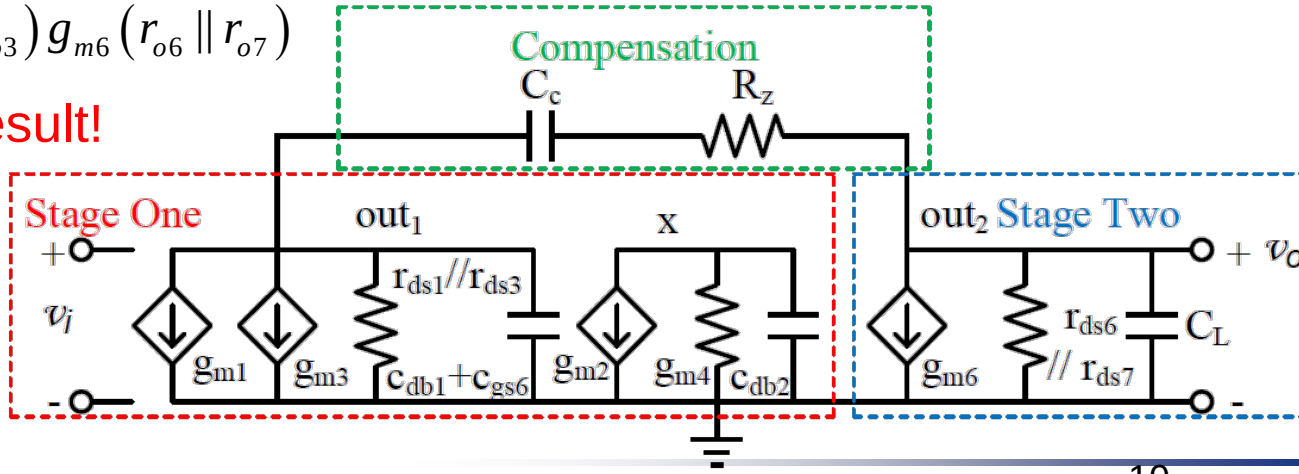




Simplified circuit

$$A_v = A_{v1}A_{v2} = -g_{m1}\left(r_{o1} \| r_{o3}\right) g_{m6}\left(r_{o6} \| r_{o7}\right)$$

Matches textbook result!



Poles & Zeros Results

- Poles & Zeros comparison for two-stage opamp

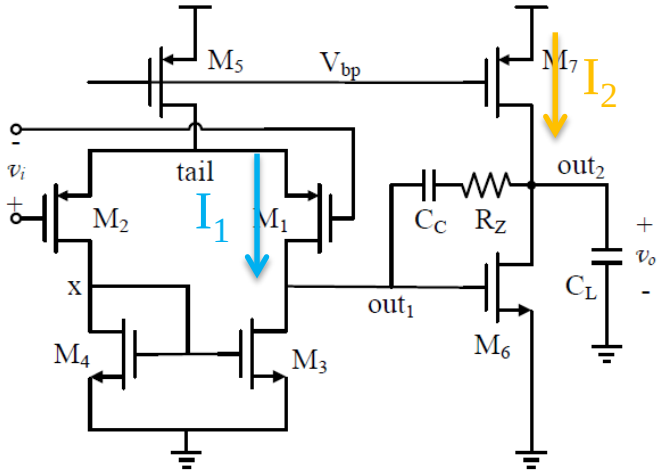
Type	Original Circuit (Hz)	Low-order Model (Hz)
Poles	-24.6K	-25.6KHz
	-19.4M	
	-374.1M±65.1M	-375.8MHz
Zeros	-21.2M	
	-298.0M	-298.1M

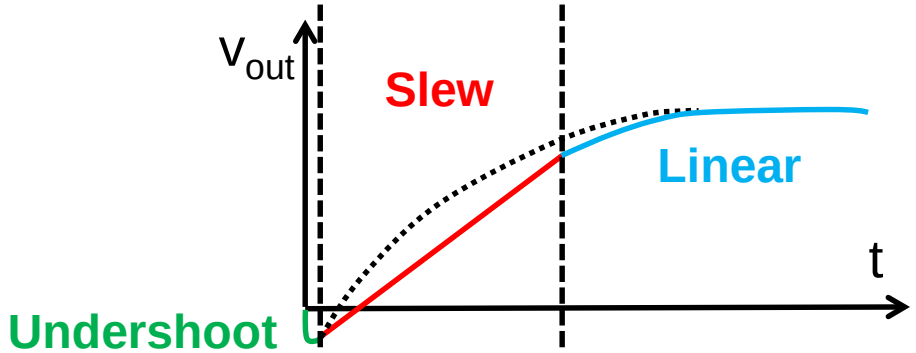
- Model order comparison

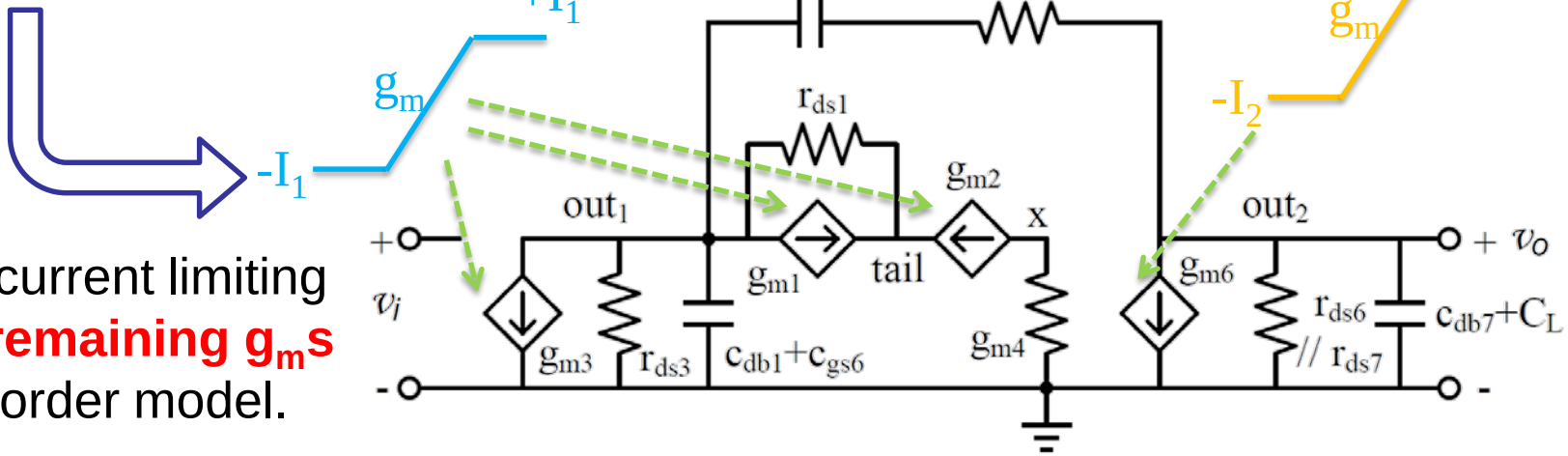
Circuit Types	Original Circuits		Low-order Models	
	# poles	# zeros	# poles	# zeros
Folded-Cascode	9	8	3	1
2-stage with nulling resistor	6	6	4	2
2-stage with voltage buffer	6	6	3	2
2-stage with current buffer	7	7	4	2

Time-Domain Model Review

- Slew-Settling Behavior



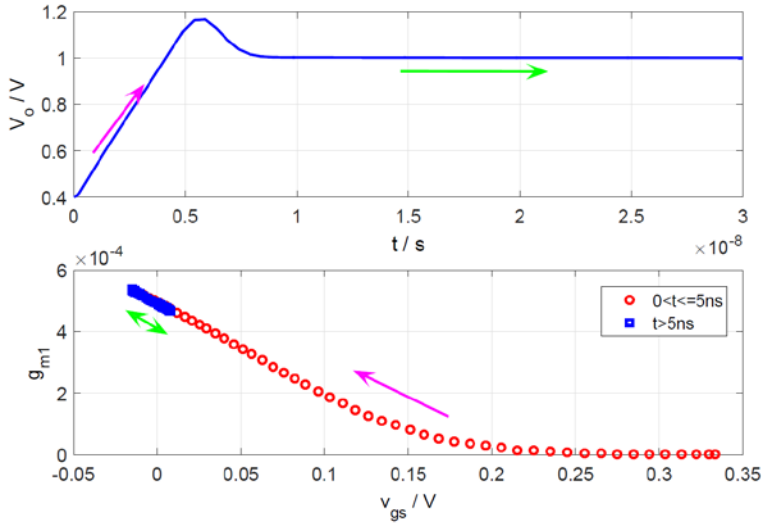




Apply the current limiting to **all the remaining g_ms** in the low-order model.

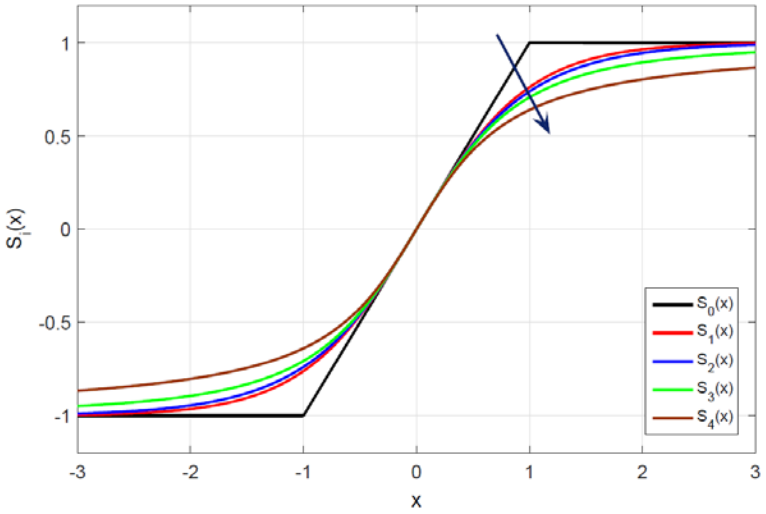
Nonlinear Function Selection

- Varying gm during the slew process



For previous works on slew-settling model, g_m was assumed zero during the entire slewing period. Actually, g_m hikes gradually as the MOSFET gate-source voltage rises by degrees.

- Sigmoid Function



$$S_0(x)=\begin{cases}1 & x\geq 1\\ x & -1\leq x<1\\ -1 & x<1\end{cases}$$

$$S_1(x)=\tanh(x)$$

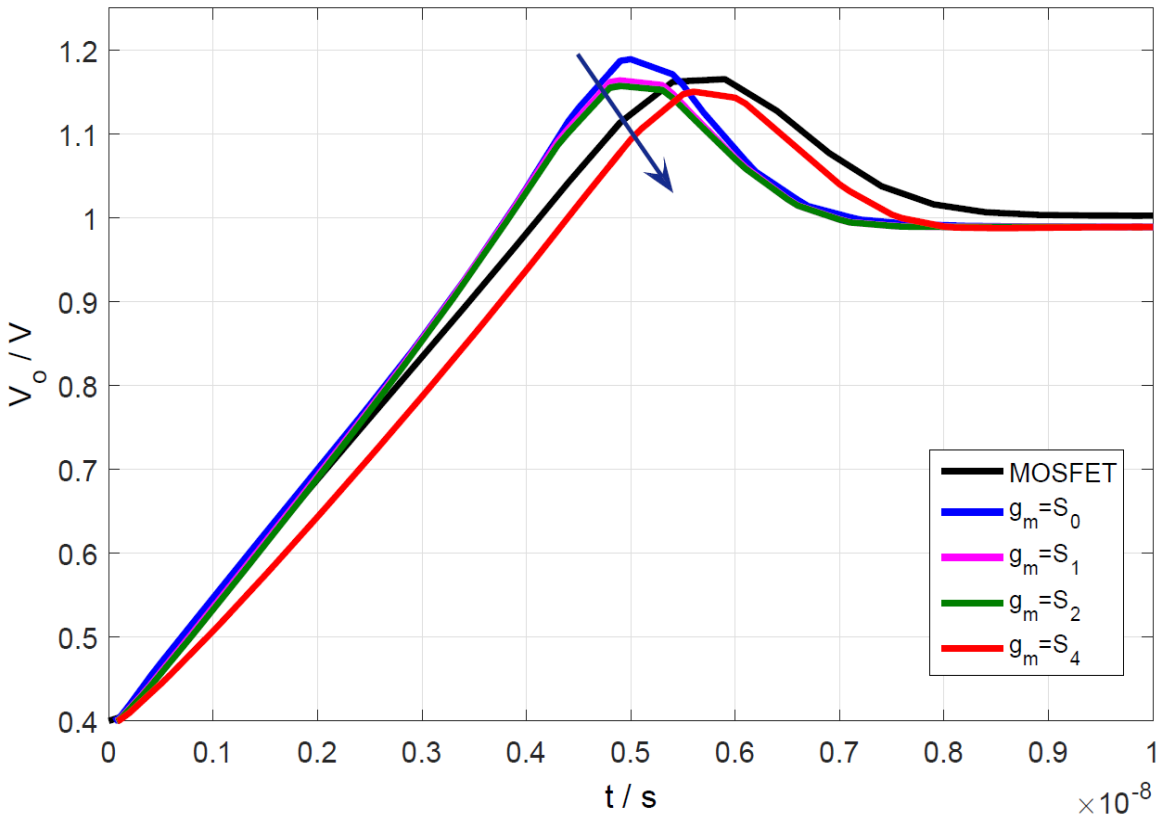
$$S_2(x)=\frac{2}{\pi}gd\left(\frac{\pi}{2}x\right)=\frac{2}{\pi}\arcsin\left(\tanh\left(\frac{\pi}{2}x\right)\right)$$

$$S_3(x)=\frac{x}{\sqrt{1+x^2}}$$

$$S_4(x)=\frac{2}{\pi}\arctan\left(\frac{\pi}{2}x\right)$$

Experimental Results

- Output voltage with different sigmoid functions



The arrow exhibits the same order as shown in the previous slide.

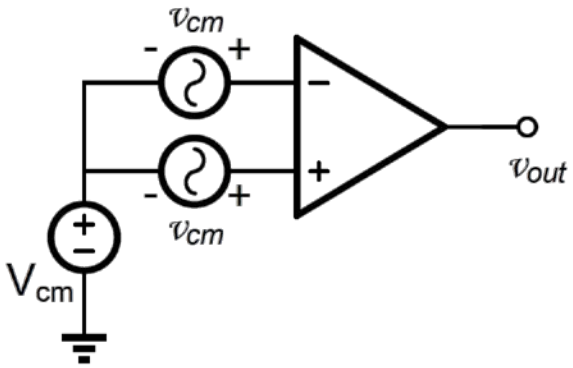
S_0, S_1, S_2 all have better performance in slew rate estimation, however, S_4 has a good agreement with transistor-level simulation in settling time prediction.

S3 is promising in both regions, but S_3 can't converge in HSPICE simulation.

CMRR/PSRR Analysis

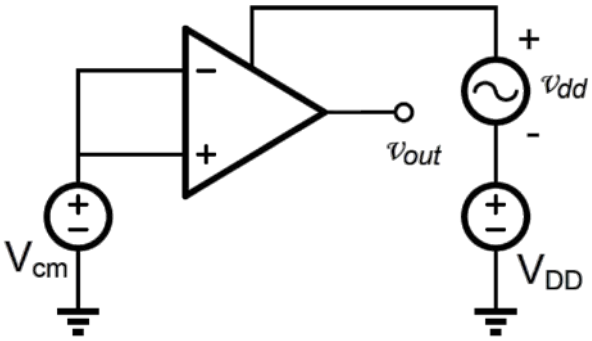
Introduction to CMRR & PSRR

CMRR: Common Mode Rejection Ratio PSRR: Power Supply Rejection Ratio



$$A_{CM} = \frac{\upsilon_{out}}{\upsilon_{cm}}$$

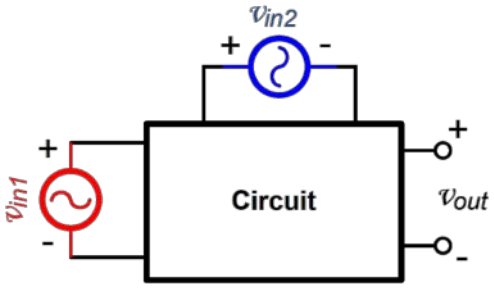
$$CMRR = \frac{A_v}{A_{CM}}$$

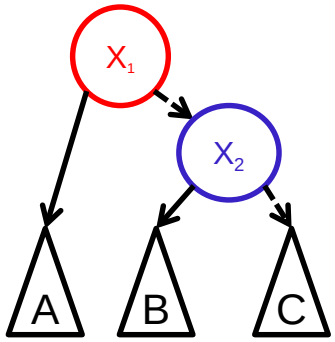


$$A_{DD}\,|_{v_{in}=0} = \frac{\upsilon_{out}}{\upsilon_{dd}}$$

$$PSRR = \frac{A_v\,|_{v_{dd}=0}}{A_{DD}\,|_{v_{in}=0}}$$

GPDD Multiport Construction





$$H_1(s) = f_A(A) \Big/ f_C(C)$$

$$H_2(s) = f_B(B) \Big/ f_C(C)$$

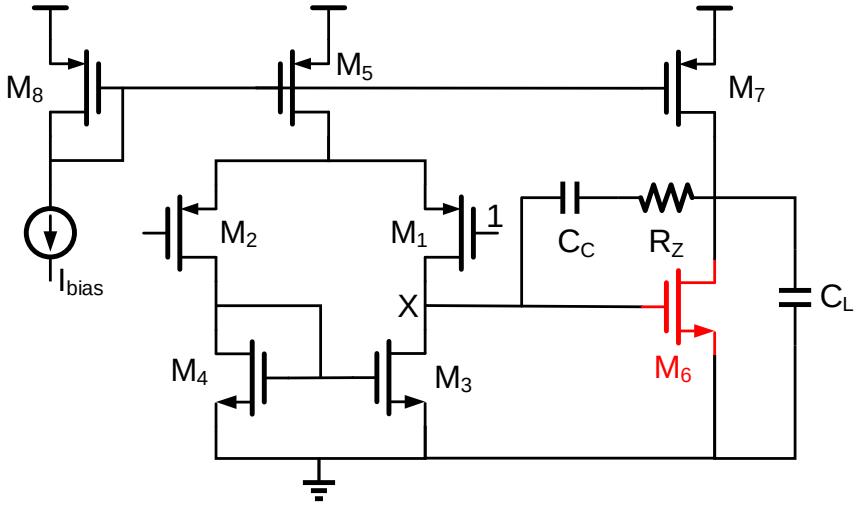
Multi-port Analysis for Opamp Sizing

W_6 Sizing

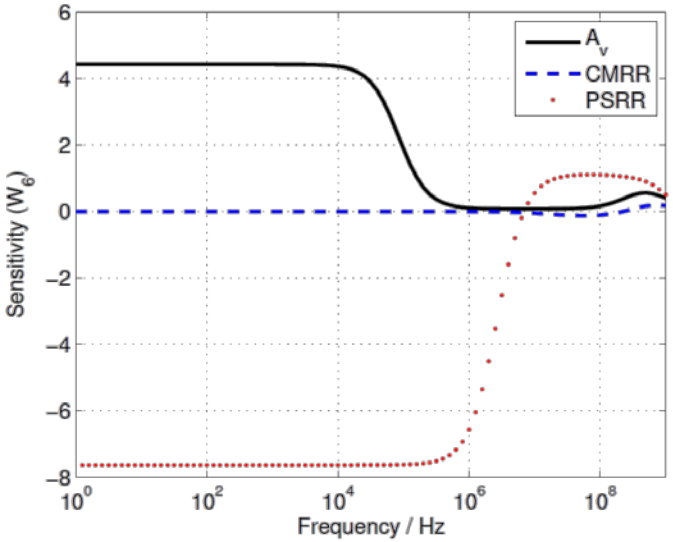
$$Sens\left(\left|H(s)\right|, W_6\right) > 0 \rightarrow W_6 \uparrow \Rightarrow \left|H(s)\right| \uparrow$$

$$Sens\left(\left|H(s)\right|, W_6\right) < 0 \rightarrow W_6 \uparrow \Rightarrow \left|H(s)\right| \downarrow$$

$$Sens\left(\left|H(s)\right|, W_6\right) = 0 \rightarrow W_6 \updownarrow \Rightarrow \overline{\left|H(s)\right|}$$



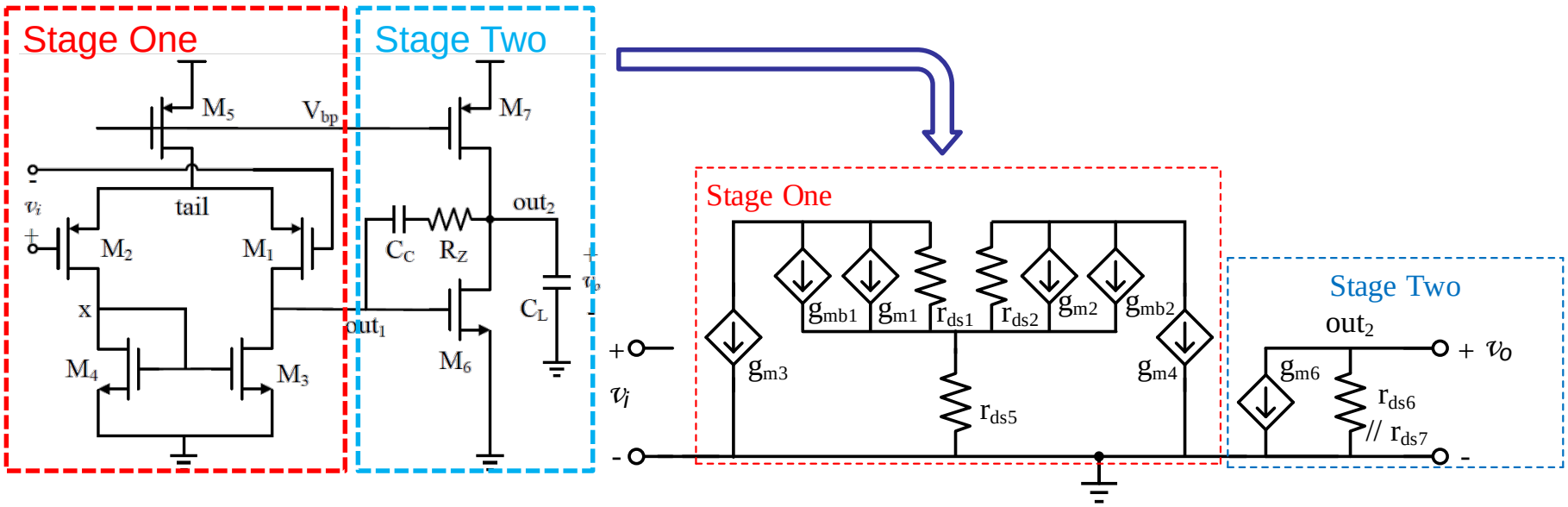
Sensitivity at DC	W_6=30um	W_6=31um	Improve
A_V	2.84K (69.1dB)	3.04K (69.7dB)	+7.04% (+0.6dB)
CMRR	2.07K (66.3dB)	2.07K (66.3dB)	+0% (+0dB)
PSRR	3.87K (71.8dB)	3.32K (70.4dB)	-14.2% (-1.4dB)
Sens(Av, W_6)	4.43	-0.20	-
Sens(CMRR,W_6)	6.1e-8	9.4e-8	-
Sens(PSRR,W_6)	-7.63	-2.83	-



Model Generation for Common Mode Gain

- Same procedure applied to common-mode gain A_{cm}
- Significance Selection (Only consider A_{cm} for now)

Original A_{cm}	Simplified A_{cm}
3.99dB	4.07dB



Conclusion

- GPDD symbolic construction can be applied to **topological circuit reduction**.
- Can automatically generate small-signal model as **behavioral model** for system-level use.
- Extended to generate large-signal model for slew-settling analysis
- Explored the possibility for multi-port model generation on GPDD.

Thanks!
Q & A