Topological Symbolic Simplification for Analog Design

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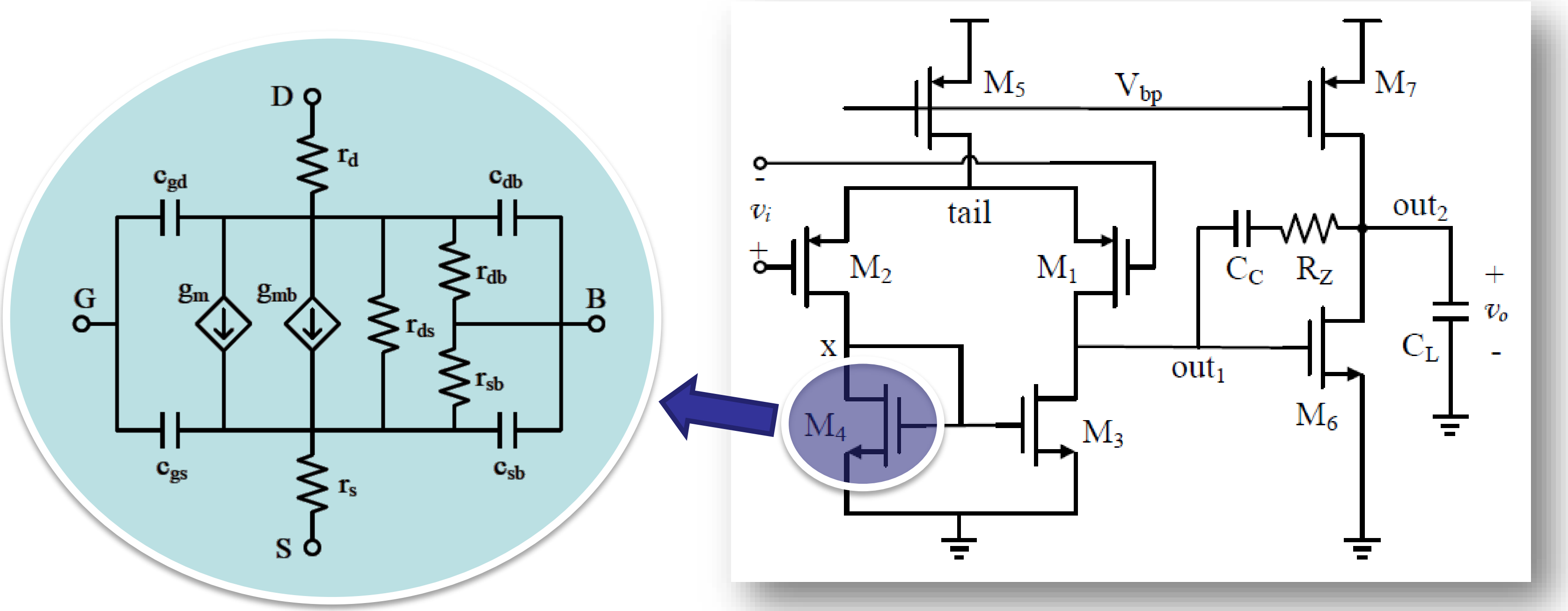
ISCAS 2015, Lisbon, Portugal, May 25-27, 2015

Outline

- Research motivation
- Background review
- **Contribution**
  - Application of symbolic topology representation to topology simplification
  - Strategy for ordering symbol significance
  - Demonstration of the effectiveness of symbolic reduction
- Experimental results
- Conclusion

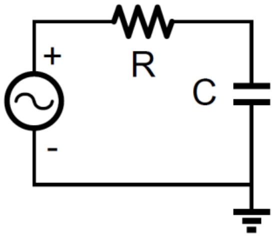
Motivation for Topology Simplification

- **Lumped small-signal model is popular in analog circuit design.**
  - **Direct symbolic analysis generates non-interpretable results.**
  - **Simplification helps deriving circuit insight** and visualizing **dominant** circuit components

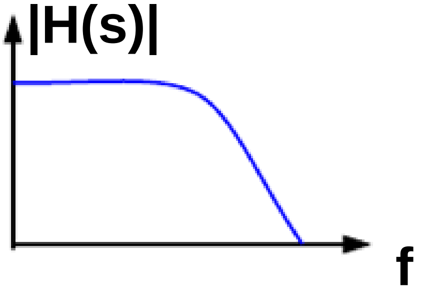


Symbolic Analysis for Simplification

- **Symbolic analysis** can generate the symbolic **circuit transfer functions**



$$H(s) = \frac{1}{1 + sRC}$$

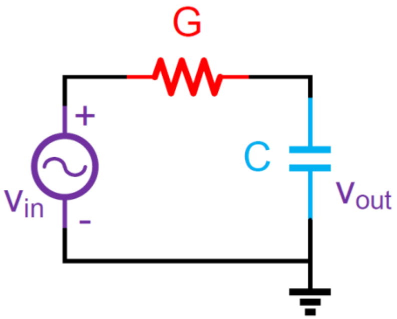


  - **Reusable**
  - **but suffers** from **exponentially growing complexity** (in circuits size)

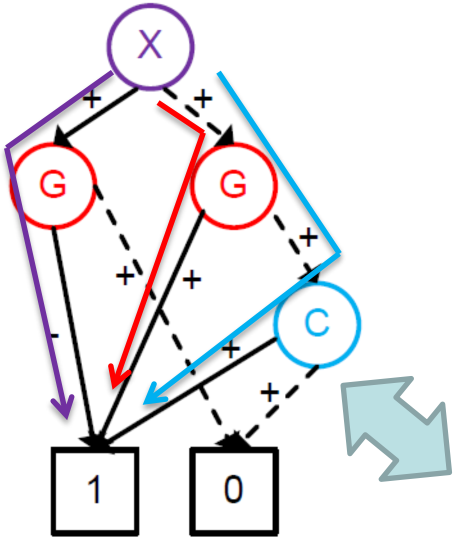
- **Symbolic simplifications** are commonly used: **SBG**, **SDG**, **SAG**.
  - Simplification “**Before / During / After”** Generation
  - Previous research in this area emphasizes **simplifying symbolic expressions, rather than topology**

A Symbolic Method capable of Handling Topology

- Graph-Paired Decision Diagram (GPDD) – A BDD
- A topology-based analysis method



Construct



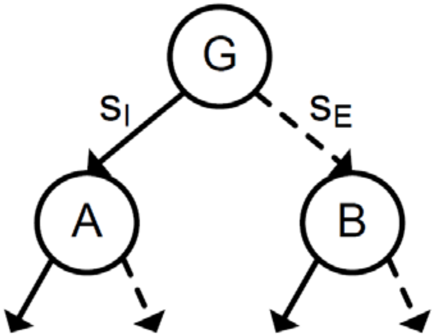
This diagram actually encodes the circuit topology

Paths in the GPDD are symbolic terms

$$-XG + G + sC = 0$$

$$\Rightarrow H(s) = \frac{1}{X} = \frac{G}{G + sC}$$

GPDD evaluation rule:



$$f_G(G) = s_I f_A(A) G + s_E f_B(B) \quad s_I, s_E = \pm 1$$

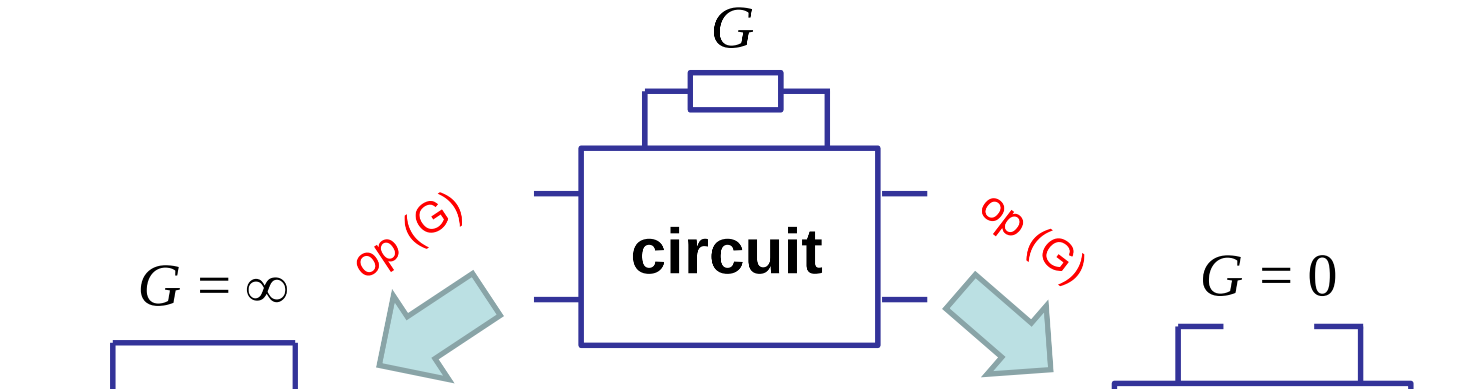
G. Shi (TCAD, 2013)

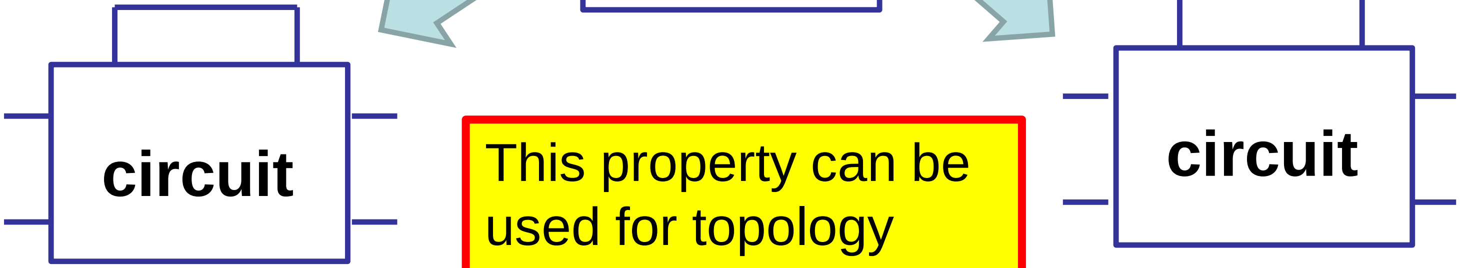
Feature of Symbols in GPDD

$$\mathrm{H(s)} = \frac{f_A(A)G + f_B(B)}{f_C(C)G + f_D(D)}$$

The numerator and denominator are **affine functions** of an arbitrary symbol; “G” in this example.

“G” taking 0 or ∞ results in two different **reduced circuits**:





Branch short

This property can be used for topology simplification!

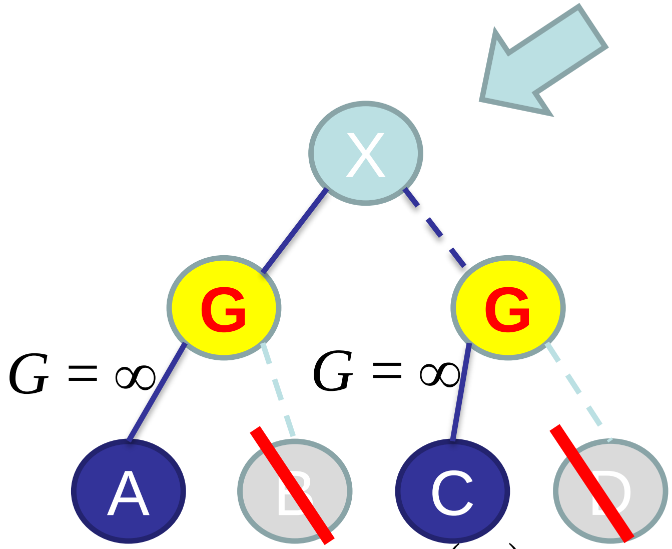
Branch open

Taking Element Limits in GPDD

- Setting a symbol to 0 or ∞ can be manipulated directly in GPDD! -- (just tracing along different paths)

$$\mathrm{H(s)} = \frac{f_A(A)G + f_B(B)}{f_C(C)G + f_D(D)}$$

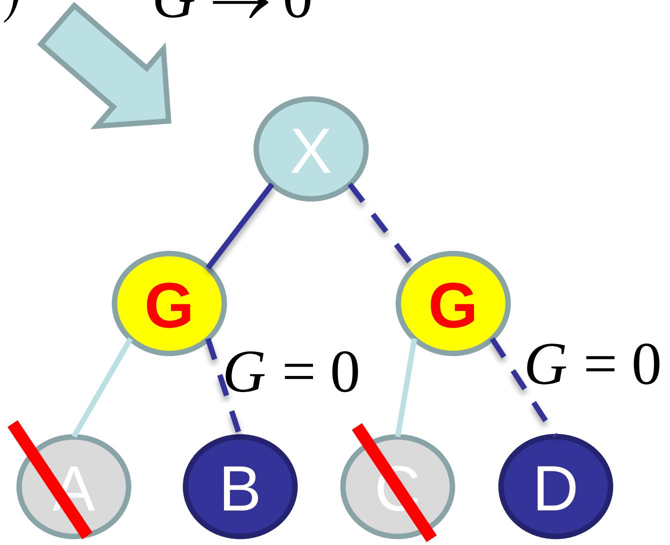
$G \rightarrow \infty$



$$\mathrm{H(s)} = \frac{f_A(A)}{f_C(C)}$$

Simplified ckt-1

$G \rightarrow 0$

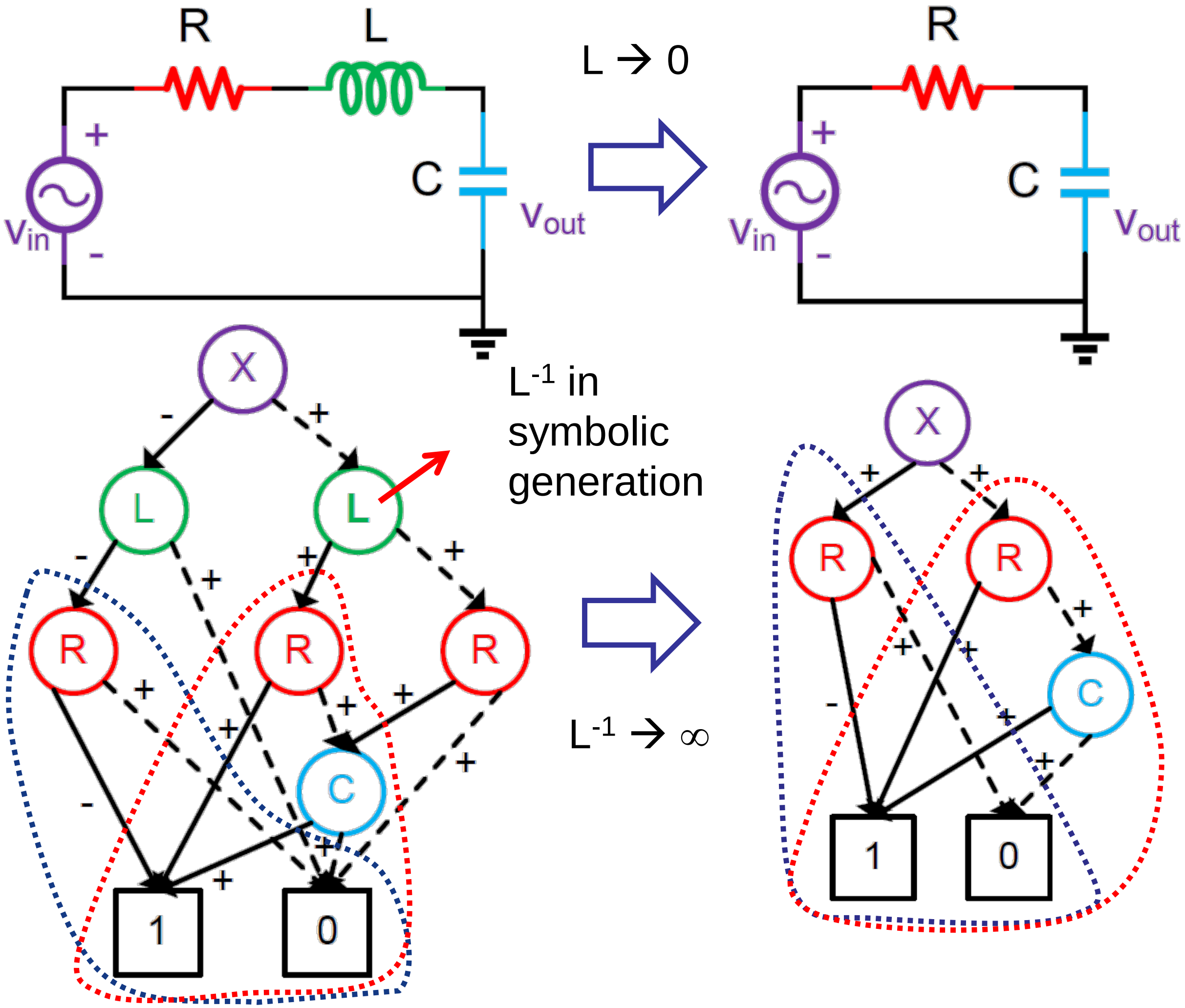


$$\mathrm{H(s)} = \frac{f_B(B)}{f_D(D)}$$

Simplified ckt-2

Example

- Reducing symbol L from an RLC circuit



L → 0

L^{-1} in symbolic generation

L^{-1} → ∞

Comments:

Obtaining GPDD for the reduced ckt is straightforward.

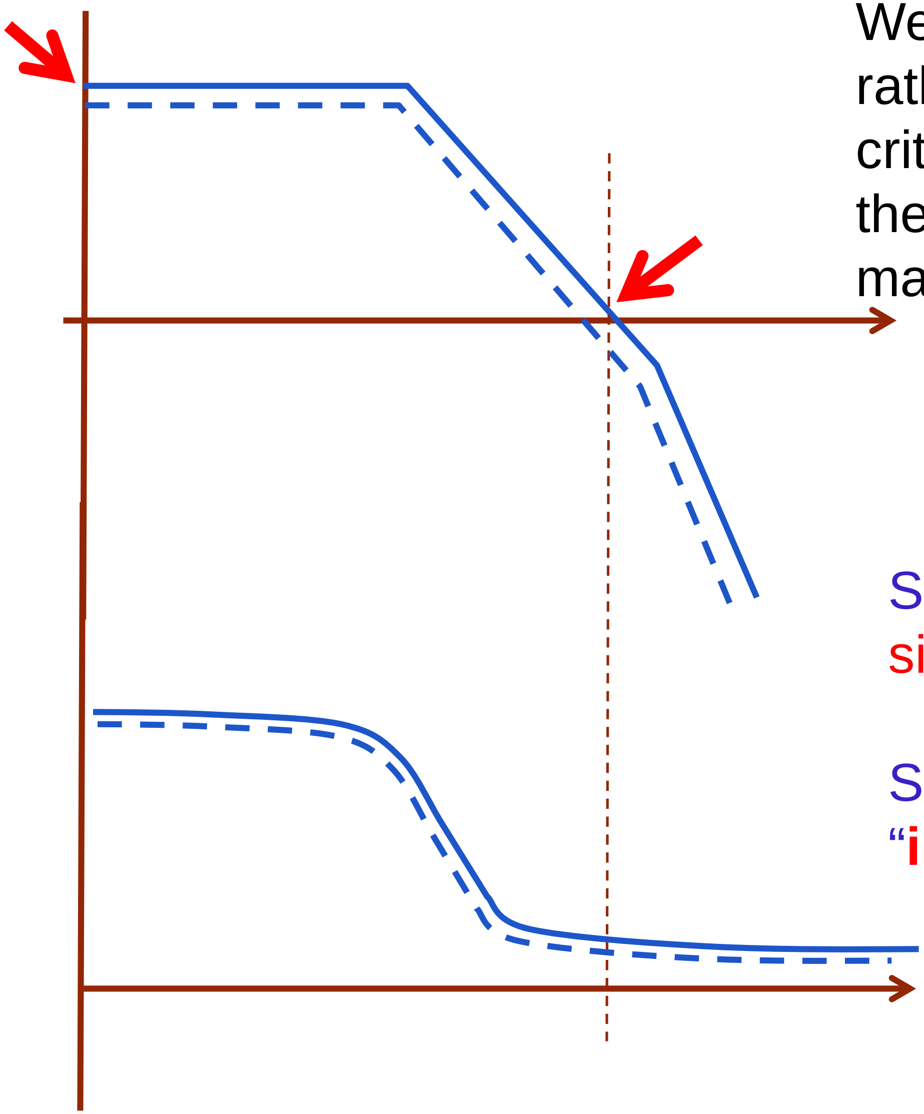
GPDD is a good media for topological circuit reduction.

Main Contributions of this Work

- Proposal of GPDD based reduction scheme
  - Done!

- An assessing method for assigning significance to each circuit element
  - “significance” to be defined later
  - Sorting element by their significance
  - Removing those least significant elements

Feature of Frequency Response



We DO NOT use sensitivity; rather we monitor several critical points of AC response – the **DC point** and the phase margin **(PM) point**.

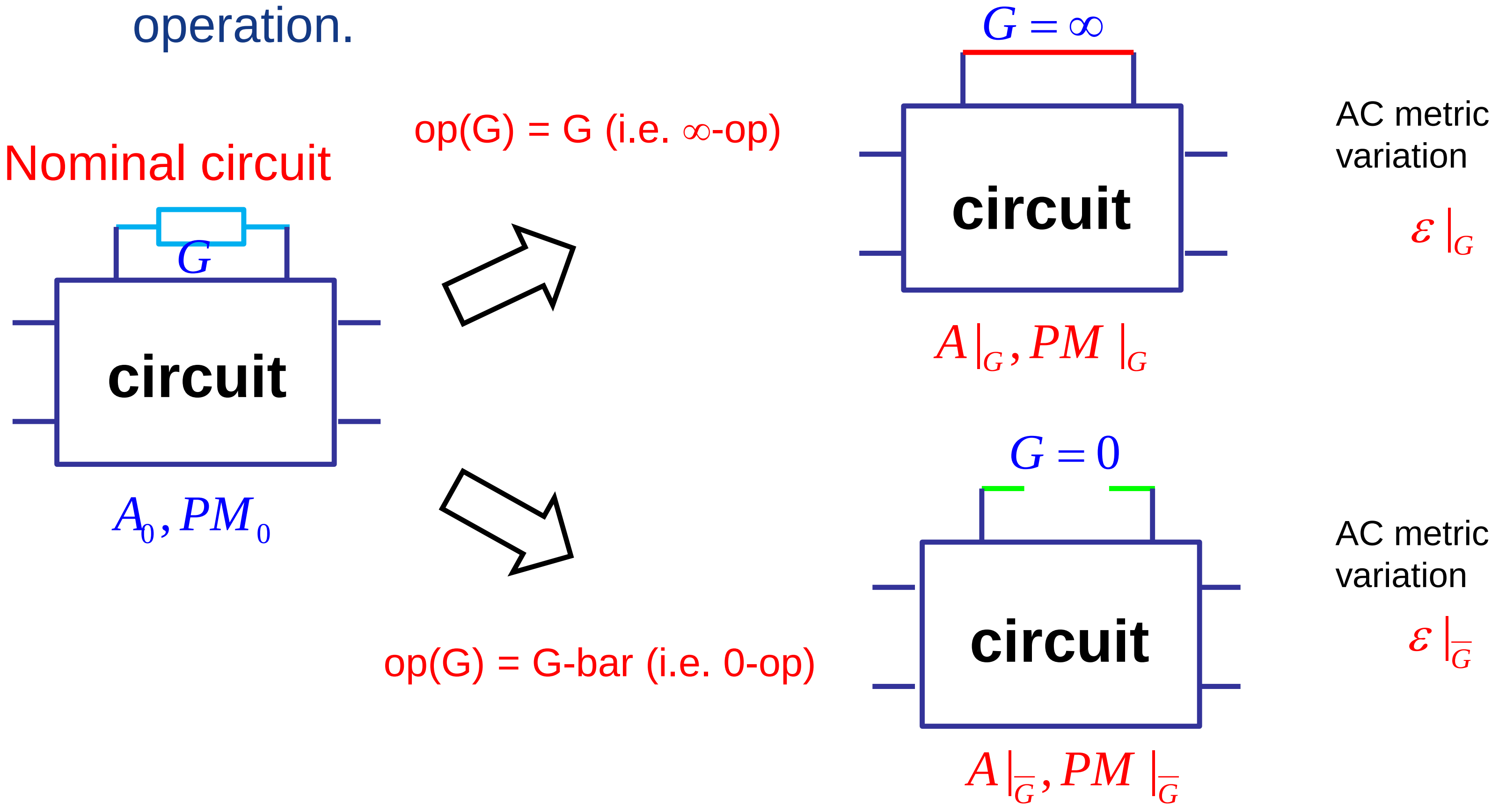
Symbols with least variation of significance can be eliminated.

Such symbols are called "**insignificant symbols**".

Significance Assessment

Definition of Symbol Significance :

- The total (relative) variation of two monitored quantities when a selected element (say, G) is operated with 0-operation or ∞-operation.



Nominal circuit

op(G) = G (i.e. ∞-op)

op(G) = G-bar (i.e. 0-op)

AC metric variation

$\varepsilon|_G$

AC metric variation

$\varepsilon|_{\bar{G}}$

Symbol Operation & Metric Variation

$$\varepsilon|_G = \sqrt{\left(\frac{A|_G - A_0}{A_0}\right)^2 + \left(\frac{PM|_G - PM_0}{PM_0}\right)^2}$$

op(G) = G
(short G)

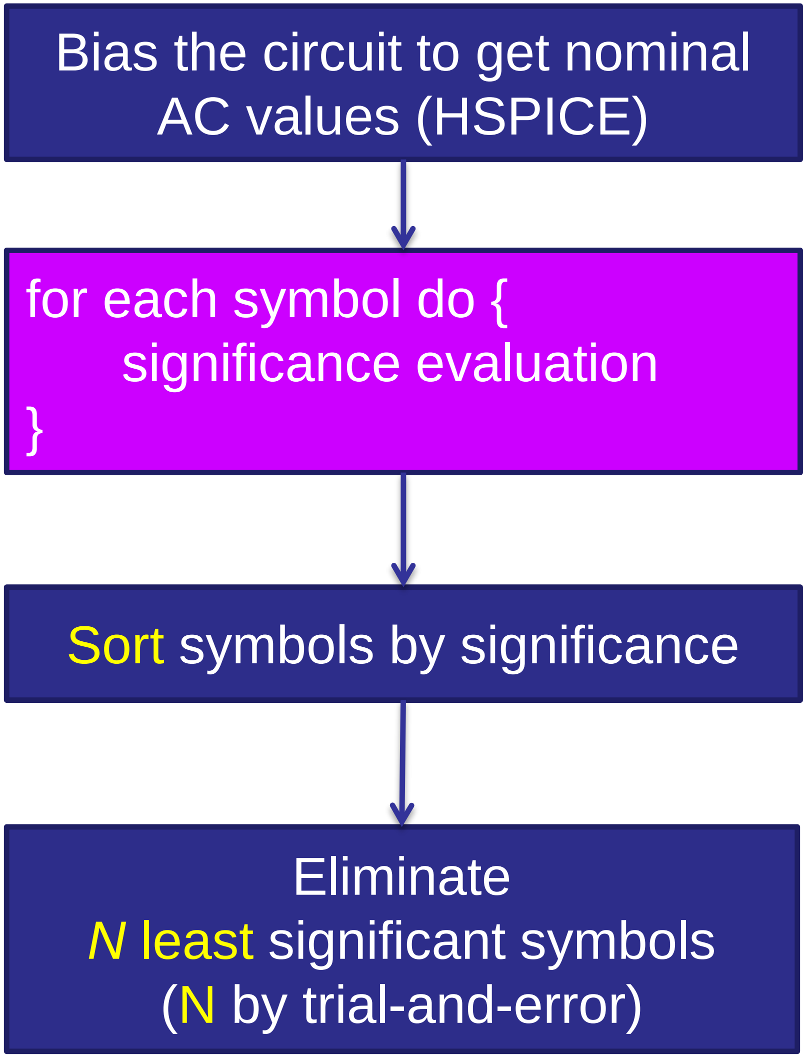
$$\varepsilon|_{\overline{G}} = \sqrt{\left(\frac{A|_{\overline{G}} - A_0}{A_0}\right)^2 + \left(\frac{PM|_{\overline{G}} - PM_0}{PM_0}\right)^2}$$

op(G) = G-bar
(open G)

Significance: $E_{op(G)} = \min\left\{\varepsilon|_G, \varepsilon|_{\overline{G}}\right\}$ **op(G) = G or G-bar**

Choose the operation with smaller metric variation

Simplification Flow



Bias the circuit to get nominal AC values (HSPICE)

```
for each symbol do {
        significance evaluation
}
```

Sort symbols by significance

Eliminate
N least significant symbols
(N by trial-and-error)

Comments on the Flow

- The symbolic GPDD is **constructed only once** for each circuit,
- and **repeatedly used** in significance evaluation for all symbols.

- The **complexity** for the significance evaluation of all symbols is proportional to the size of GPDD x num of symbols in the circuit.
  - Several seconds in our experiment

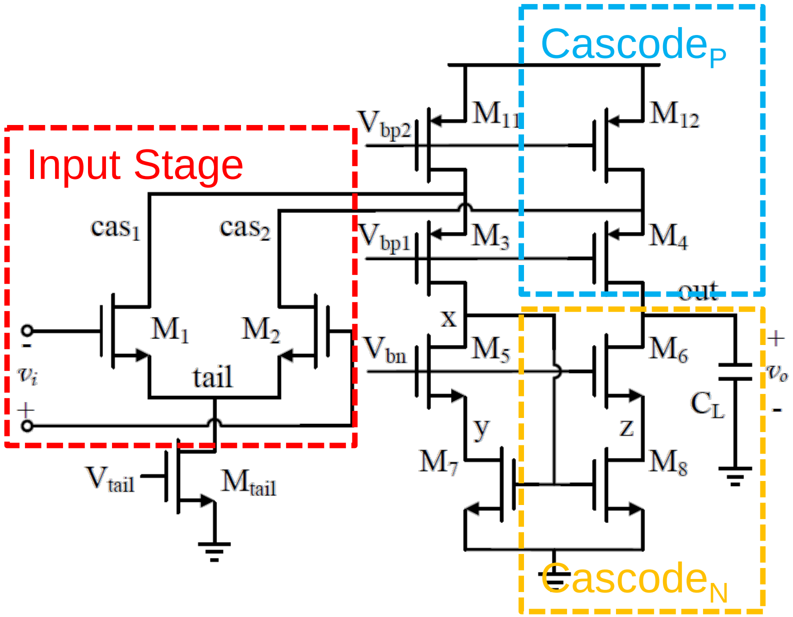
Experimental Results

Test Circuit 1

Folded-cascode opamp

Observations:

1) Topological structure preserved
2) Virtual ground (tail) preserved



Reduction from 123 symbols to 18 symbols in 3.9 seconds

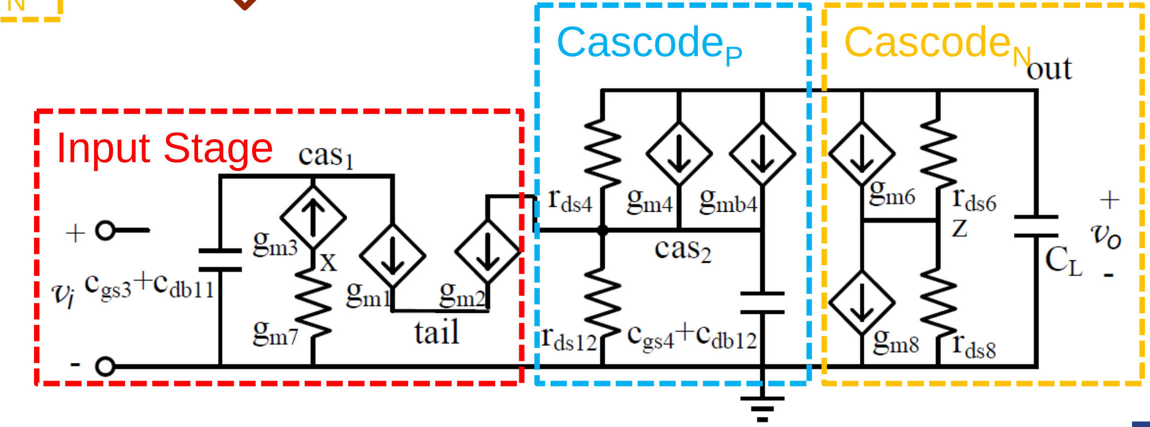
$$A_v = G_m R_o = -g_{m1}\left[\left(R_{out,4}\right)\|\left(R_{out,6}\right)\right]$$

$$R_{out,4} = \left[g_{m4}\left(r_{ds2}\|r_{ds12}\right)\right]r_{ds4}$$

$$R_{out,6} = \left(g_{m6}r_{ds8}\right)r_{ds6}$$

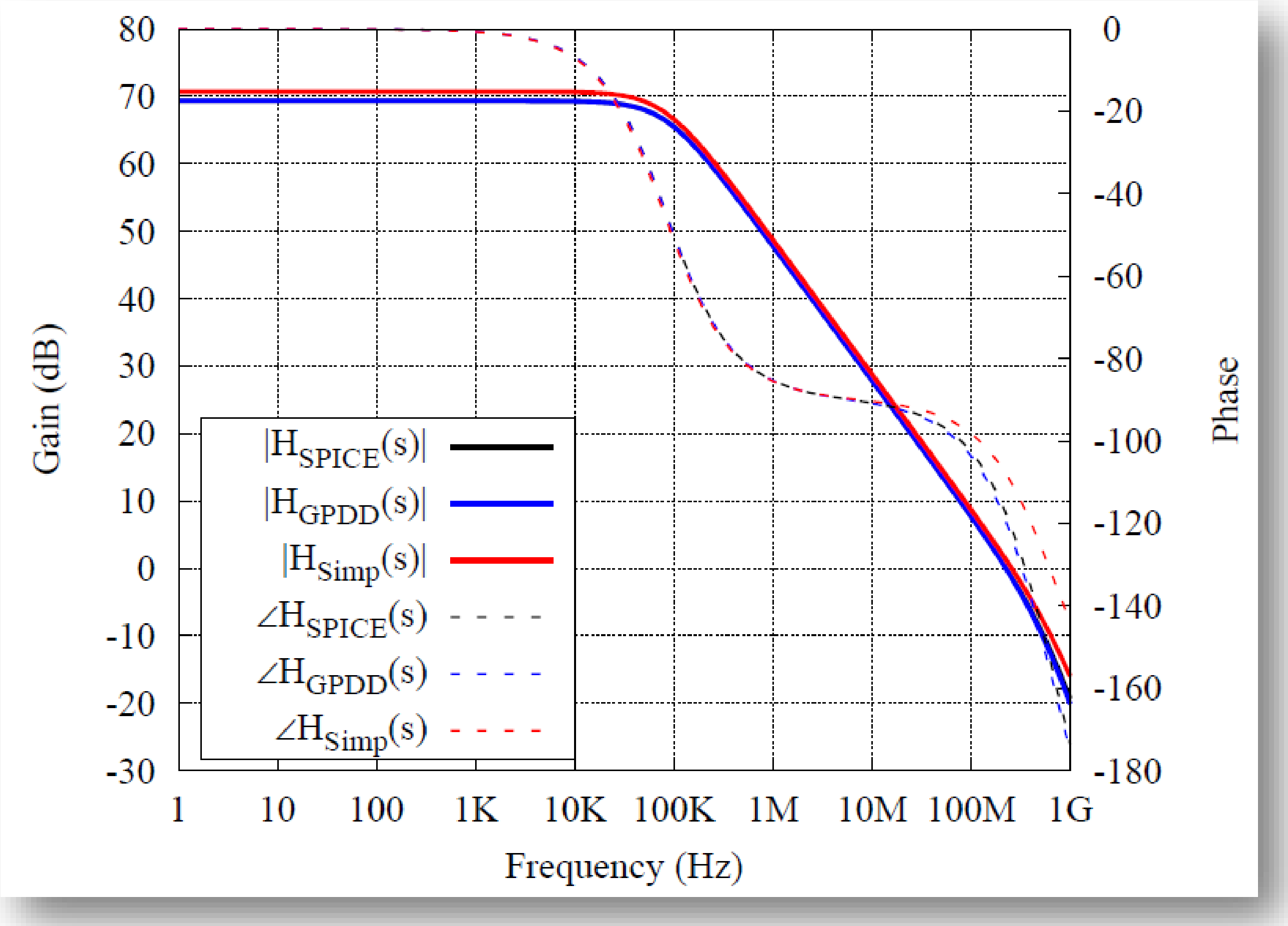
Matches textbook result!

Simplified circuit



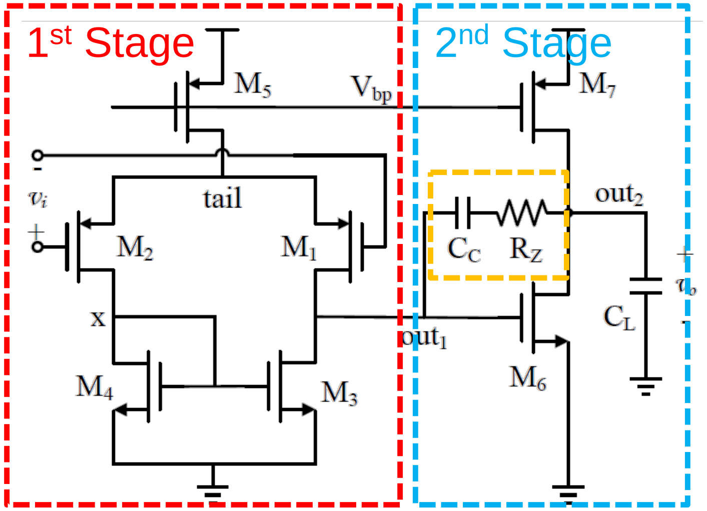
Test Circuit 1 (cont'd)

Check the frequency response (comparing full ckt, reduced ckt, and SPICE results)



Test Circuit 2

Two-stage opamp



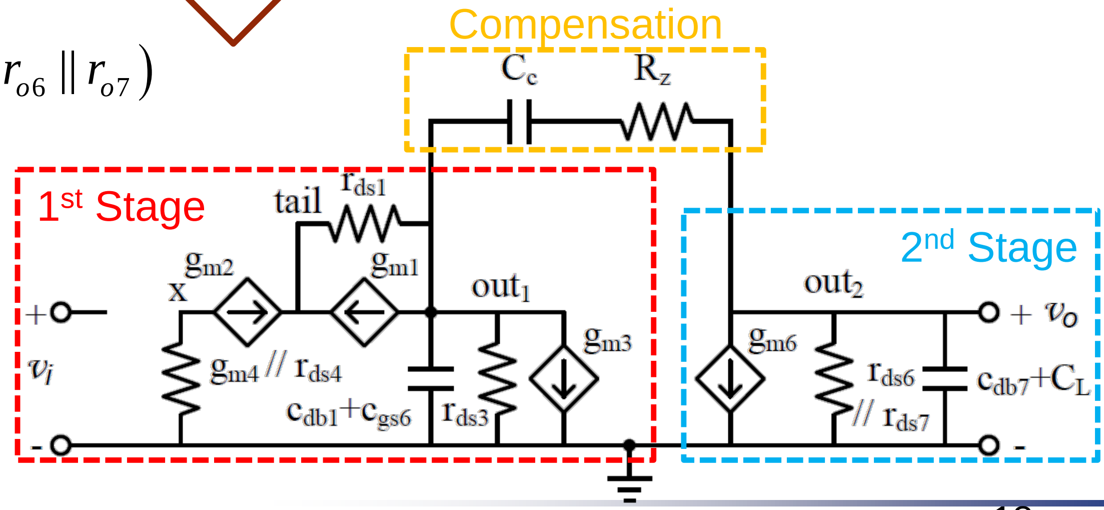
$$A_v = A_{v1}A_{v2} = -g_{m1}\left(r_{o1} \| r_{o3}\right) g_{m6}\left(r_{o6} \| r_{o7}\right)$$

Observations:

1) Two-stage structure preserved
2) Compensation preserved
3) Virtual ground (tail) preserved

Reduction from 81 symbols to 16 symbols in 0.1 seconds

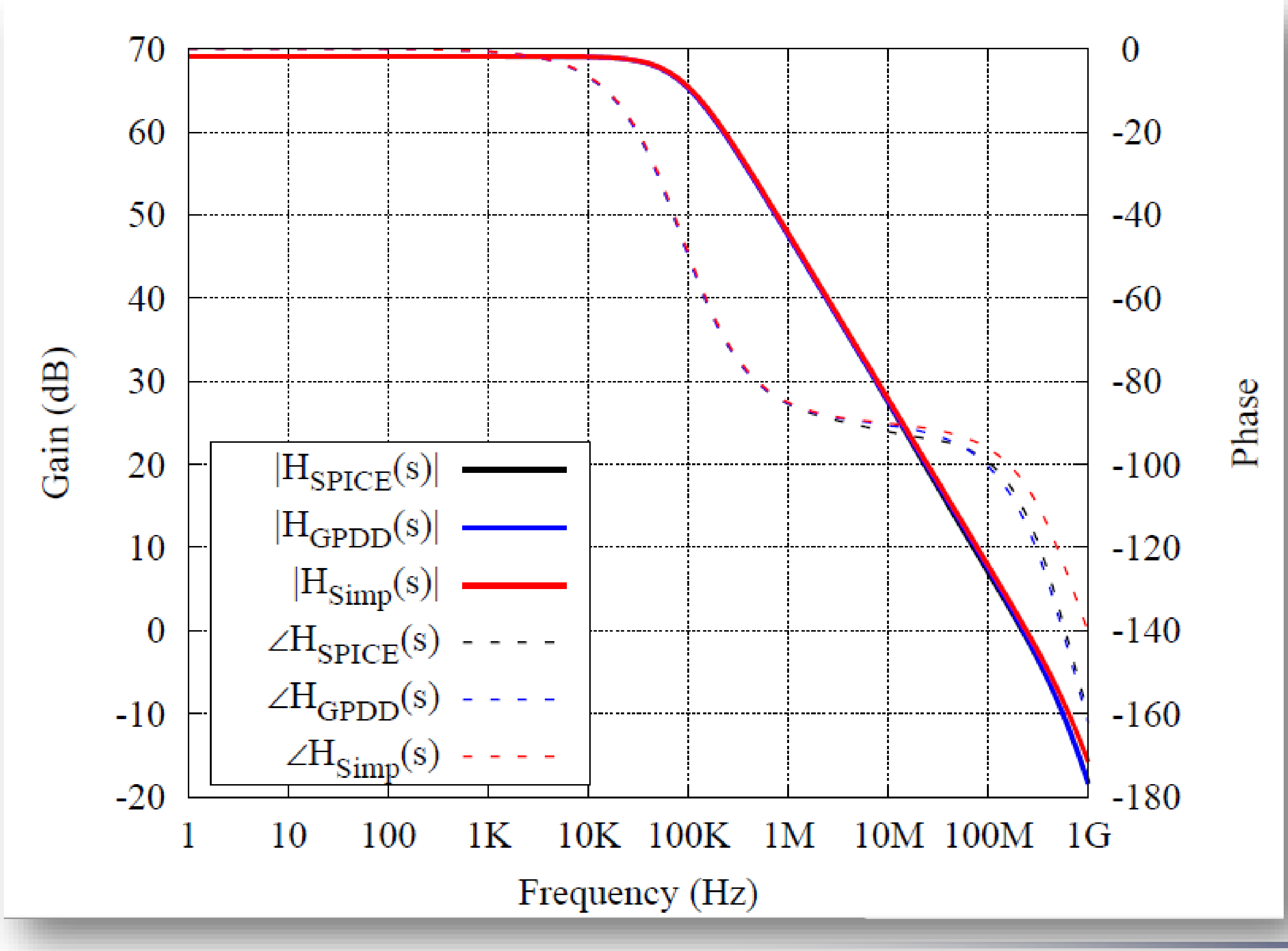
Simplified circuit



Matches textbook result!

Test Circuit 2 (cont'd)

Check the frequency response (comparing full ckt, reduced ckt, and SPICE results)



Further Study

- Improving the assessment metrics
  - Incorporating other design metrics (CMRR and PSRR, ...)
- Robustness of generated models
  - Extensible to slew-settling model
  - Help extraction of symbolic dominant poles/zeros
- Graphical interface support - for readable schematic

- Automatically determine the **num of symbols to eliminate**

Conclusion

- GPDD symbolic construction can be applied to topological circuit reduction.
- Can automatically generate small-signal model as behavioral model for system-level use.
- Can be extended to generate large-signal model for slew-settling analysis
  - Future work

Thanks!
Q & A