A Low Voltage Low Power Sigma Delta Modulator Design

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***Abstract*—Bio-medical electronics have made great progress in the past decade. Data converter plays an important role in the whole system, which enables sampling the analog signal from the real world and processing the signal in a stable, fast and simple manner in digital domain. In this work, a discrete-time sigma-delta modulator is presented with low power consumption and sufficient resolution in purpose of ECG signal sampling for pacemaker application. A bulk-driven OTA with 0.8V supply voltage is employed in the whole system, applying the self-cascode technique.**

***Index Terms*—Sigma-Delta Modulator, low voltage, bulk-driven.**

I. Introduction

Bio-medical electronics have made great progress in the past decade. Data converter plays an important role in the whole system, which enables sampling the analog signal from the real world and processing the signal in a stable, fast and simple manner in digital domain. However, the critical problem of bio-medical electronic design is power consumption, which involves the convenience and safety issue in practical application.

There are numerous kinds of Analog-Digital Converter(ADC), such as Flash ADC and Pipeline ADC. Sigma-Delta ADC, also named as Sigma-Delta Modulator(SDM), acquire the high precision with low working frequency, differing from other types of ADC. [1] Due to the simple structure, Sigma-Delta Modulator is much easier to achieve less power consumption [2], which dominates in bio-medical electronic design.

This work intended to realize a sigma-delta modulator for pacemaker application, which means relatively low requirements on signal bandwidth and resolution. However, it demands low power consumption in order to implant in human body. This work combines some energy-saving designs focused on different parts of ADC to achieve relatively low power consumption. [3], [4] Section II reviews the background of Sigma-Delta Modulator. In Section III the detailed circuit implementation is explained and illustrated. Several simulation results are presented in Section IV. Section V concludes the report.

II. Review on Sigma-Delta Modulator

Most signals in nature are of analog form representing the continuous variation of physical quantities in time or in space. The processing of these signals is more effectively performed in the digital domain. The digital signal can be easily processed, transmitted, stored or converted back to analog signal, so that it could be properly detected by the real world sensors.

Analog-to-Digital Conversion can be carried out using the conventional Nyquist converters or those, which are based on other techniques. Conventional high-resolution A/D converters, such as successive approximation and flash type convertors, operating at sampling frequency approximately equal to twice the maximum frequency in the input signal, also named as Nyquist rate, often do not make use of the exceptionally high speeds achieved with VLSI technology.

The Analog-to-Digital Conversion process involves two consecutive operations on the original analog signal. The first is uniform sampling whereas the second one is uniform quantization. The implementation of these operations is carried out by means of special circuitry, which is essential in building A/D convertors. After that, the encoding follows which gives the final digital signal.

A. Oversampling

The high resolution and dynamic range requirements in modern signal processing cannot be fully satisfied by the conventional ADCs, because of limitations in their implementation. One way of improving the situation is to increase the sampling rate many times higher than that of the conventional ADCs, i.e. above the Nyquist rate $f_N = 2f_b$. Of course this requires the various components of the ADC to operate at a much higher frequency. Sampling at a higher rate f_s, higher than the Nyquist rate f_N, is called oversampling. A critical parameter of this technique is the Oversampling ratio (OSR), defined as follows:

$$OSR = \frac{f_s}{f_N} \tag{1}$$

The result of the oversampling is that the images of the signal band are not close to one another and, consequently, the specifications of the anti-aliasing filter can be relaxed. Furthermore, the quality of the digital signal, as far as the SNR is concerned, is improved when oversampling is applied. The quantization noise power is distributed in a larger frequency range. Consequently, the power of the part of the quantization noise lying in the signal is reduced. The quantization noise lying outside the signal band can be eliminated by means of a high accuracy digital filter.

B. Noise shaping

A further improvement in the SNR can be achieved by pushing also most of the in-band noise, left after the oversampling, outside the signal frequency band. This is attainable if the $STF(z)$ is all-pass whereas, and most important, the $NTF(z)$ is high-pass. This technique is called noise shaping and can be easily and efficiently implemented by modifying the Delta-Modulator system. [2] The idea is to encode the integral of the input signal rather than the input signal directly. Delta-Sigma Modulator achieves quantization noise shaping, and it pushes the quantization noise outside the signal band as it is shown in Fig. The letter Σ is signifying the fact that the input signal is integrated first before entering the delta-modulator.

C. 1st order SDM modeling

The elementary diagram of Sigma-Delta Modulator is shown in Fig 1. The input analog signal are compared with the output signal, and the difference between them are integrated and then quantized to digital output. The feedback loop is called *Loop Filter*, which determines the order of the modulator and the signal-to-noise ratio (SNR) performance. In addition, Sigma-Delta Modulator takes advantage of *oversampling* and *noise shaping* techniques to gain high precision with a low-bit quantizer.

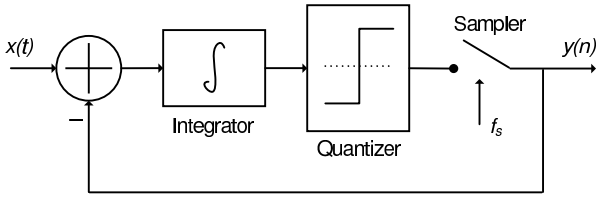

Fig. 1. Sigma Delta Modulator Principle

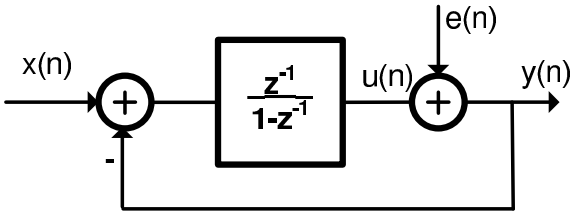

Fig. 2. 1st order Sigma Delta Modulator model

The first-order SDM employs oversampling to spread the quantization noise over the $[0, f_s/2]$ frequency band, as well as noise shaping. The block diagram of sigma-delta-modulator is shown in Fig 2. while for the sake of analysis its linear model is shown in fig. The sampler and the encoder are omitted as they have no impact on the analysis at this level, while the quantizer is replaced by its linear model.

By straightforward analysis of the linear system in Fig 2, we can easily obtain the following:

$$Y(z) = z^{-1}X(z) + (1 - z^{-1}E(z)) \tag{2}$$

From the equation above, the STF and the NTF are

$$STF(z) = z^{-1} \tag{3}$$

$$NTF(z) = 1 - z^{-1} \tag{4}$$

Clearly, the $STF(z)$ leaves the signal unaltered, just delayed by the period of a single bit, whereas the $NTF(z)$ high-passed the quantization error, and it shapes it by suppressing it at low frequencies.

More details about Sigma-Delta Modulator are illustrated in [1], [2], [5].

III. Circuit Implementation

A. Operational Transconductance Amplifier Design

Since a low power Sigma-Delta Modulator(SDM) is required with typical SNR, the operational transconductance amplifier(OTA) should consume less current and demand high gain. A bulk-driven OTA proposed in [4] is built with self-cascode technique proposed in [6].

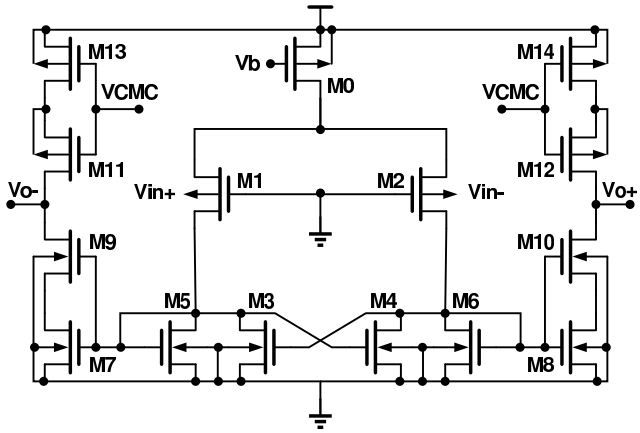

Fig. 3. Operational Transconductance Amplifier Schematic

In Fig.3, the schematic of the OTA is depicted, and it can be seen that the bulk-driven circuitry is employed. This technique is widely used in low power design due to the constant threshold voltage as the scaling down continues. [7] The potential between the source and the bulk of the transistor adjusts the threshold voltage of MOSFET, as the equation below shows.

$$V_T = V_{T0} \pm \gamma(\sqrt{2|\Phi_F| - V_{BS}} - \sqrt{2|\Phi_F|}) \tag{5}$$

This technique enables channel to be in the strong inversion when V_{gs} is 0 like a JFET with low g_m and low cutoff frequency in contrast of gate-driven approach. The method significantly improves the input range of OTA, especially in low voltage design. In order to enhance the gain and output swing of the output stage of the bulk-driven OTA, self-cascode technique is employed in this circuitry. [6] Transistor M10 is sized to work in weak inversion region to keep M8 in saturation region, which imply a large output resistance and a wide output voltage swing. [4]

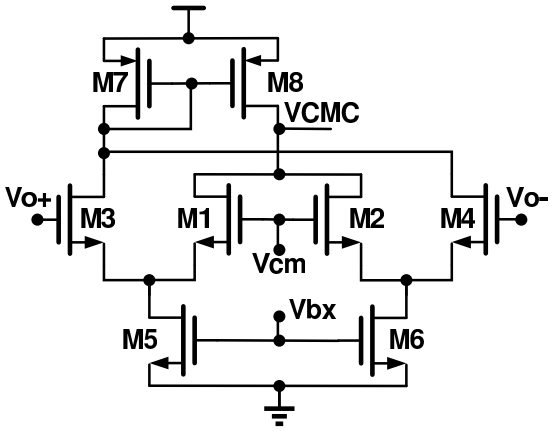

Fig. 4. Common-mode feedback topology

For the output is a differential one, the common mode output voltage is unknown. Common Mode Feedback is proposed in [8] and a traditional voltage feedback circuitry in [9] is applied in this design, shown in Fig.4. The circuitry for bias voltage and current generator is given in [10]. In order to achieve high gain and low current consumption, all the transistors should be sized sufficiently well. The performance of OTA is shown in IV.

B. Low Power Comparator Design

The comparator applied is proposed in [3], shown in Fig. 5. This comparator includes the clock signal to implement a track and latch one. There are two phase of this comparator: reset and evaluation phase. In the reset phase, two outputs are shorted to ground through transistor M9 and M10. During the evaluation phase, the comparator compares the two input voltage and get a one-bit output. In the conventional track and latch comparator, the current is flowed during all the whole evaluation phase.

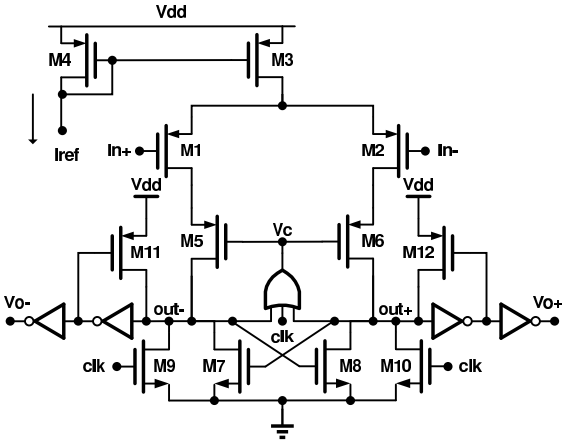

Fig. 5. Low power comparator Schematic

This design adds transistor M5 and M6 to control the flow of bias current charged by the OR gate. When the clk is high(reset phase), transistor M5 and M6 is obviously off. Otherwise, in the evaluation phase, as long as one of the two output achieves Vdd, the Vc voltage will be high to cut off M5 and M6. Thus, the current consumption only happens in the transition of the two phase, which get a high performance in power consumption.

C. Entire System

The actual implementation of whole circuitry is shown in Fig. 6. Due to the time limitation of the course, only a 1st-order SDM system is built in cadence with the process of TSMC 0.18μm CMOS technology. The whole circuit works under the voltage supply of 0.8V. The circuit also includes a clock generator to generate two-phase non-overlapping clock and bias circuit for OTA, which isn't shown in Fig. 2

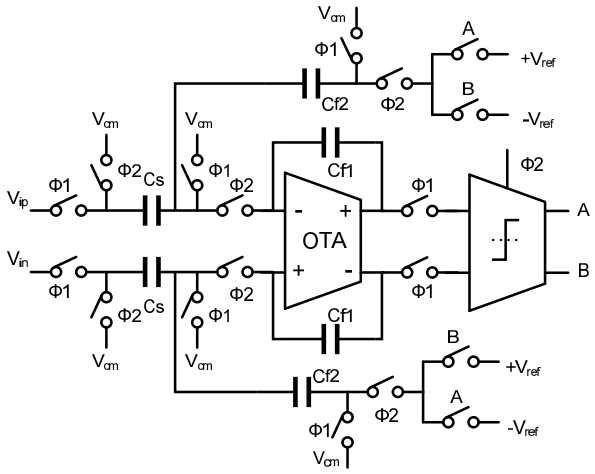

Fig. 6. Circuitry for the entire 1st-order SDM system

The entire system is built with switch-capacitor methods, which is regarded as one of the most popular approaches to construct a SDM system. Since what really matters is the ratio between these capacitors, fabrication error can be reduced if the sizes of the same group capacitors are shifted in the same direction.

IV. Simulation Results

Fig.7 is the frequency response of the OTA, and Table.I summarizes the performance of the OTA, which shows a relatively small power consumption and sufficient gain for amplifying. All the test of OTA connect a 5pF load capacitance at the output of the OTA. Both of the input and output common mode voltage is 0.4V under a supply of 0.8V.

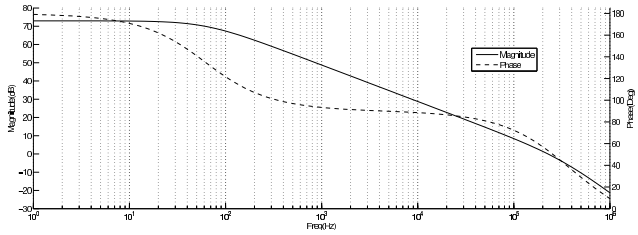

Fig. 7. Frequency Response of applied OTA

TABLE I
SUMMARY OF OTA PERFORMANCE

Characteristics	Simulated Value
Open-loop DC gain	73dB
Unity gain-bandwidth	226.6kHz
Total current consumption	431.1nA
Phase margin	53.54°
Slew rate	752.9V/ns
Process	0.18-μm CMOS
Voltage Supply	0.8V
Common Mode Voltage	0.4V

Fig. 8 shows the current consumption of the working comparator. It can be found that the current consumption only happens just at the edge of the clock signal, which doesn't consume any power during most of the evaluation time and prove the circuitry of the comparator.

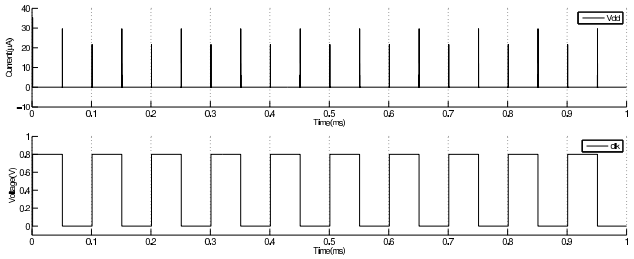

Fig. 8. Current Consumption of comparator

We still cannot give the simulation results of the whole SDM, since the power spectrum density(PSD) requires large amounts of samples, which means long simulation time in cadence. Table II shows some basic setting of the simulated sigma-delta modulator.

TABLE II
SIGMA DELTA MODULATOR PERFORMANCE

Characteristics	Simulated Value
Bandwidth	250Hz
Input signal frequency	78.125Hz
OSR	20
SNR	21.8dB
ENOB	3.33bit
VDD	0.8V
Process	TSMC 0.18-μm CMOS

V. CONCLUSION

This paper reviews the basic principle of sigma-delta modulator, and presents several low voltage low power building blocks for sigma-delta modulator. A high-gain low power OTA is constructed with 344.9nW power consumption and 73dB gain, applying bulk-driven and self-cascode technique. A track and latch comparator is also built with less power in evaluation phase. A 1st-order SDM is given due to the limited course time, and the simulated results will be presented in the presentation.

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