Incremental Symbolic Construction for Topological Modeling of Analog Circuits

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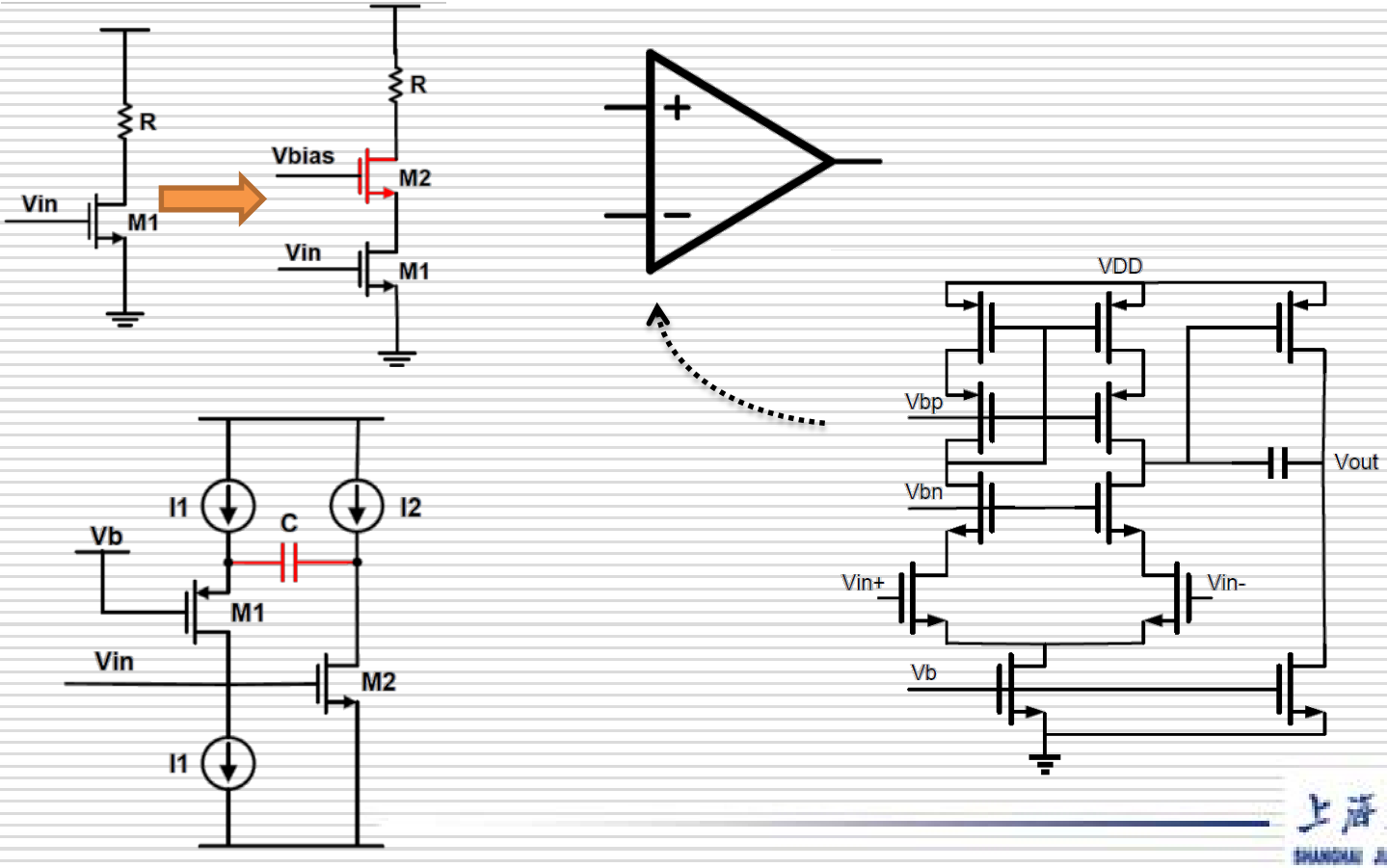
Outline

- Motivation
- Background
- Incremental Algorithm
  - Symbol Deletion
  - Symbol Insertion
- Symbol Reordering
- Conclusion

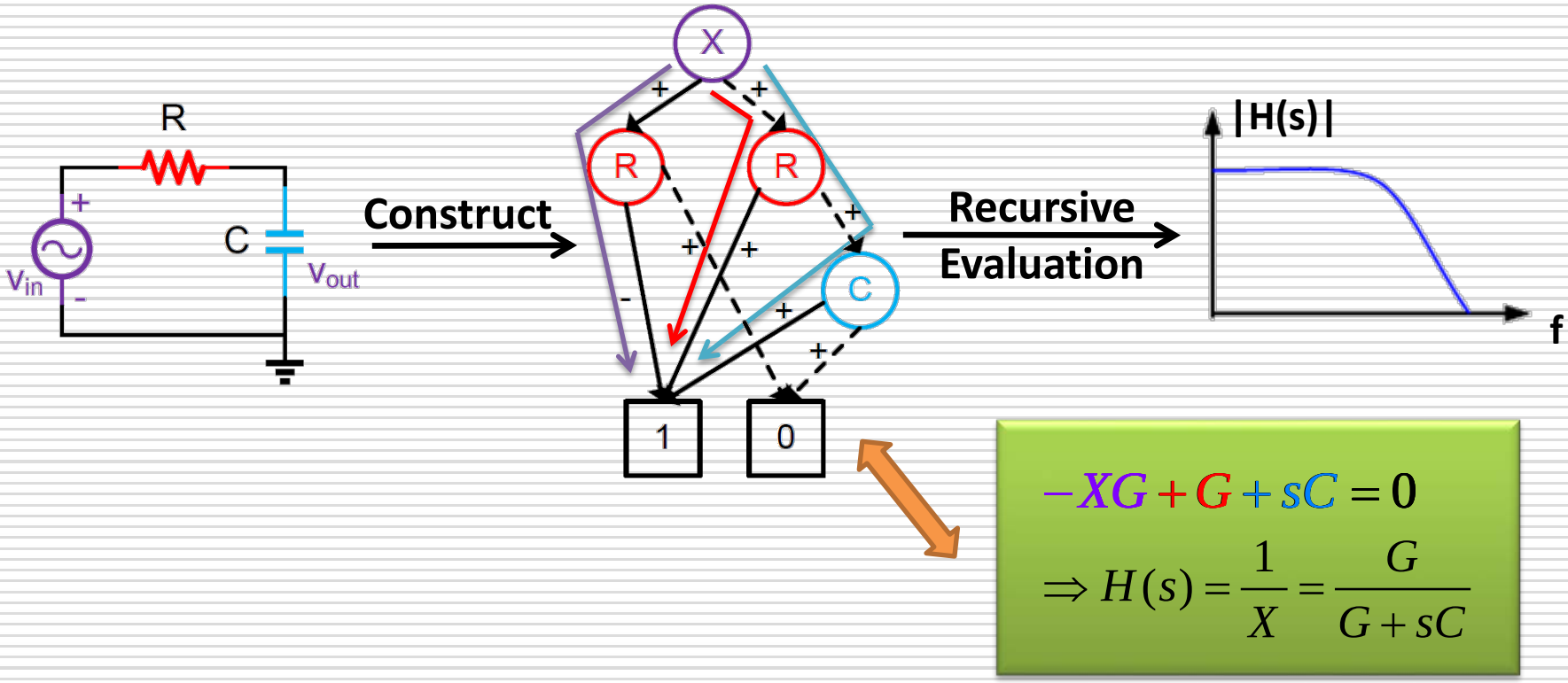
Motivation

- Topology adjustment in analog circuit design
- Difficulty in design automation



Background

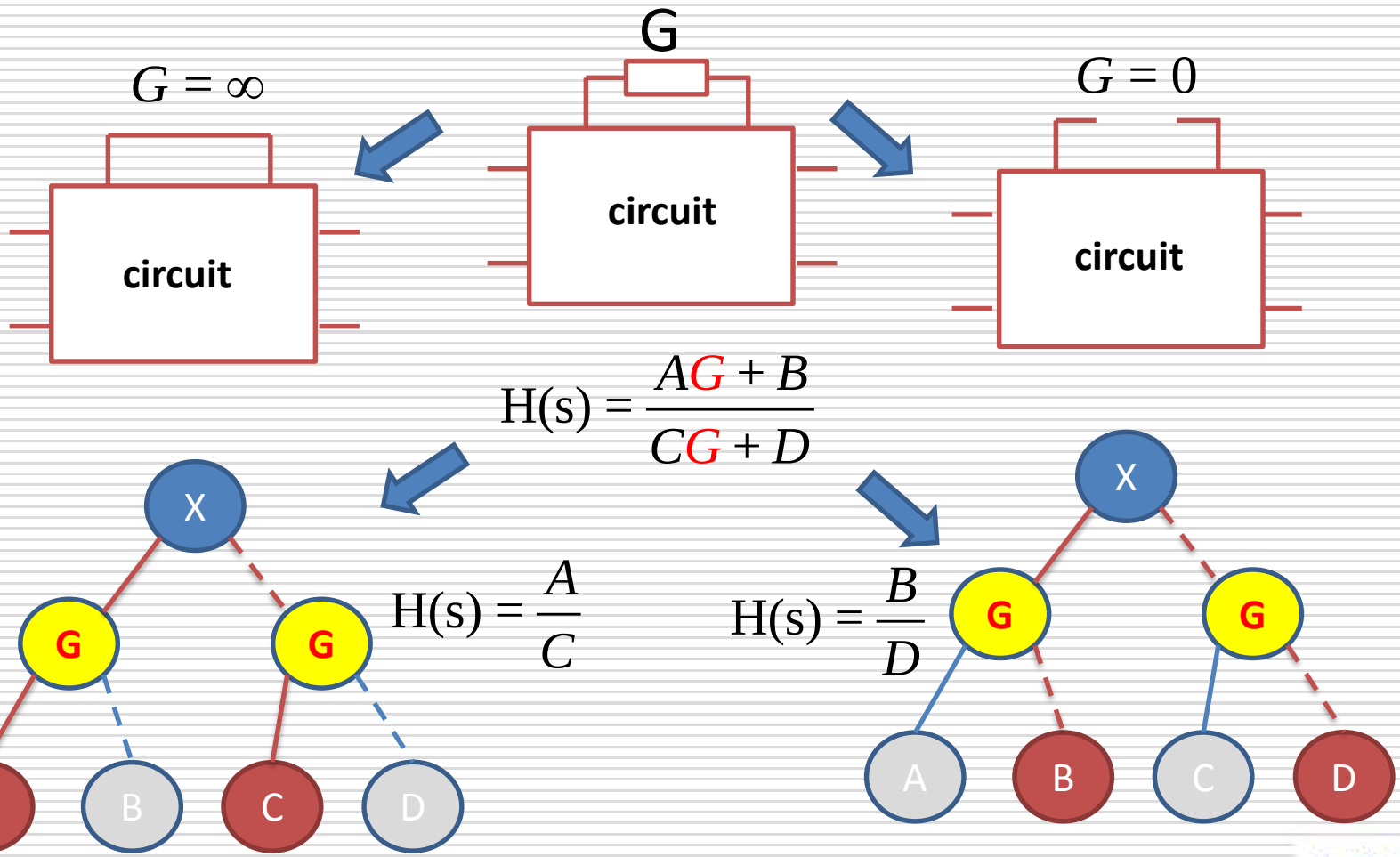
- Symbolic Analysis



[1] G. Shi, "Graph-pair decision diagram construction for topological symbolic circuit analysis," *TCAD, 2013.*

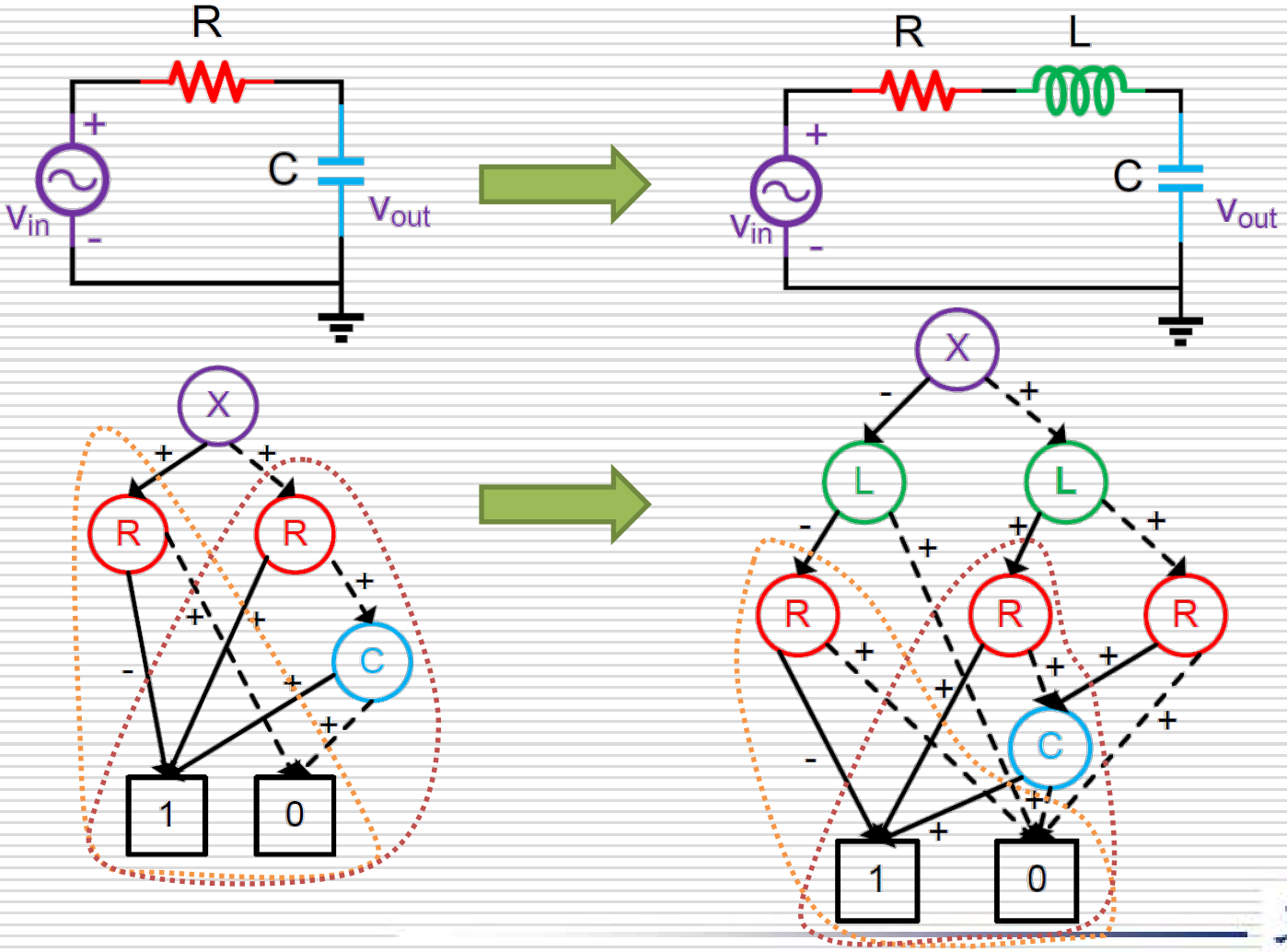
Incremental Algorithm

- Symbol Deletion (G = ∞ or G = 0)



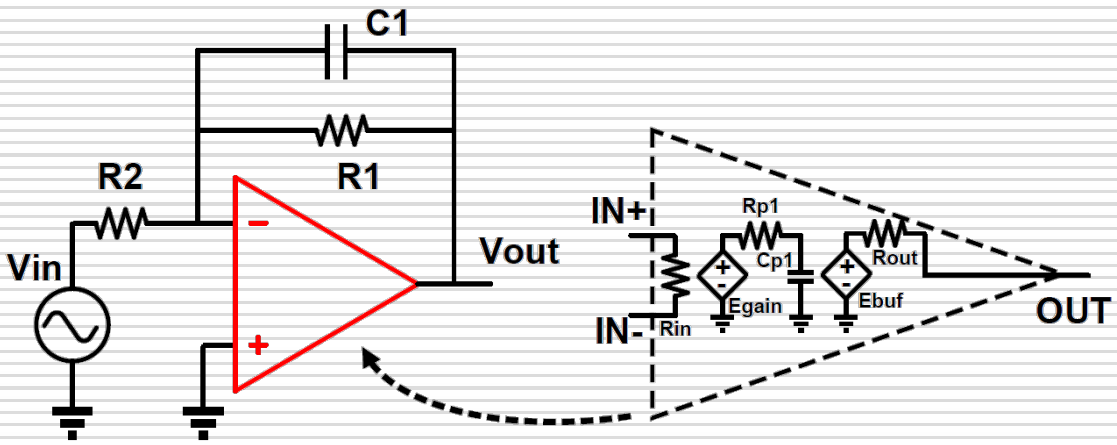
Incremental Algorithm

- Symbol Insertion Demo



Incremental Algorithm

- Test Result

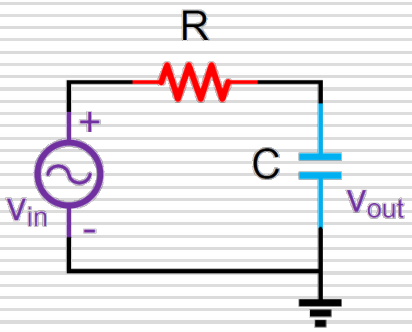


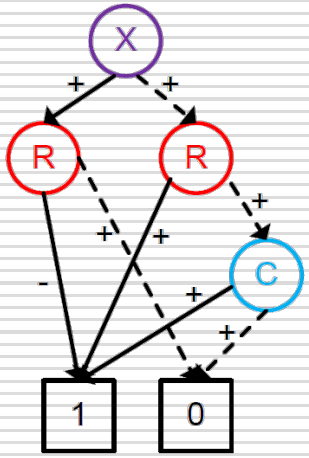
Symbol	TIME(us)	|GPDD|
Origin	976	5
Egain	34	3
Ebuf	44	4
Rin	54	2
Rout	119	5
Rp1	36	3
Cp1	259	5
$\sum$	1,522	27

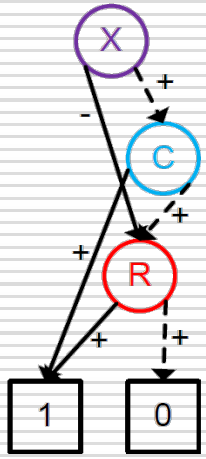
Total construction time of one-shot method is 1,736us for 21 GPDD vertex.

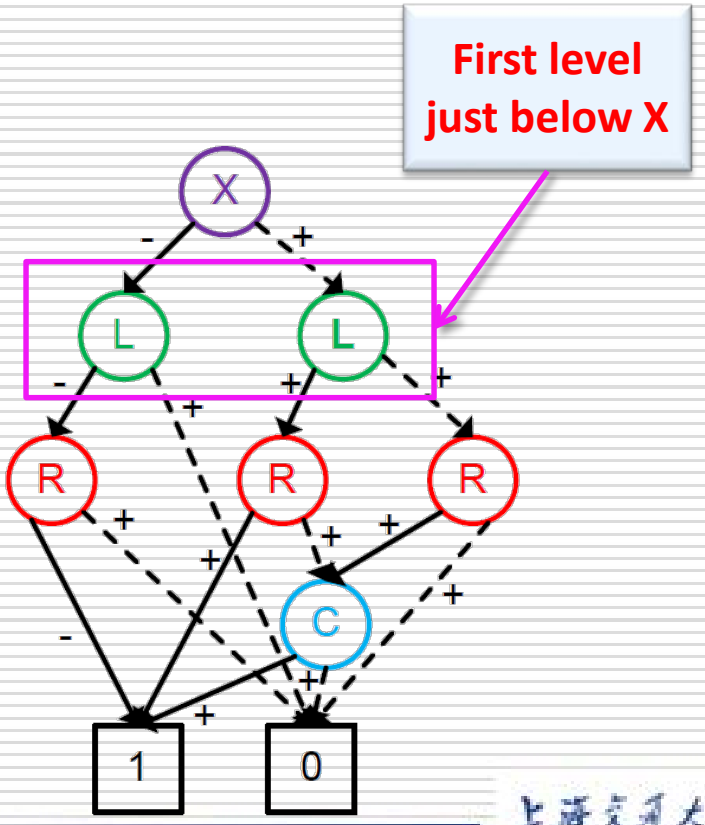
Symbol Reordering

- Symbol order effect on GPDD scale

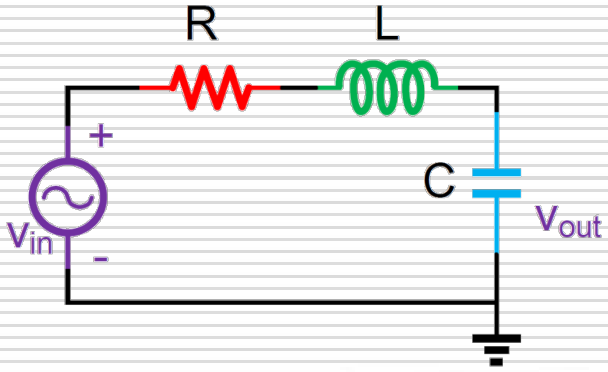






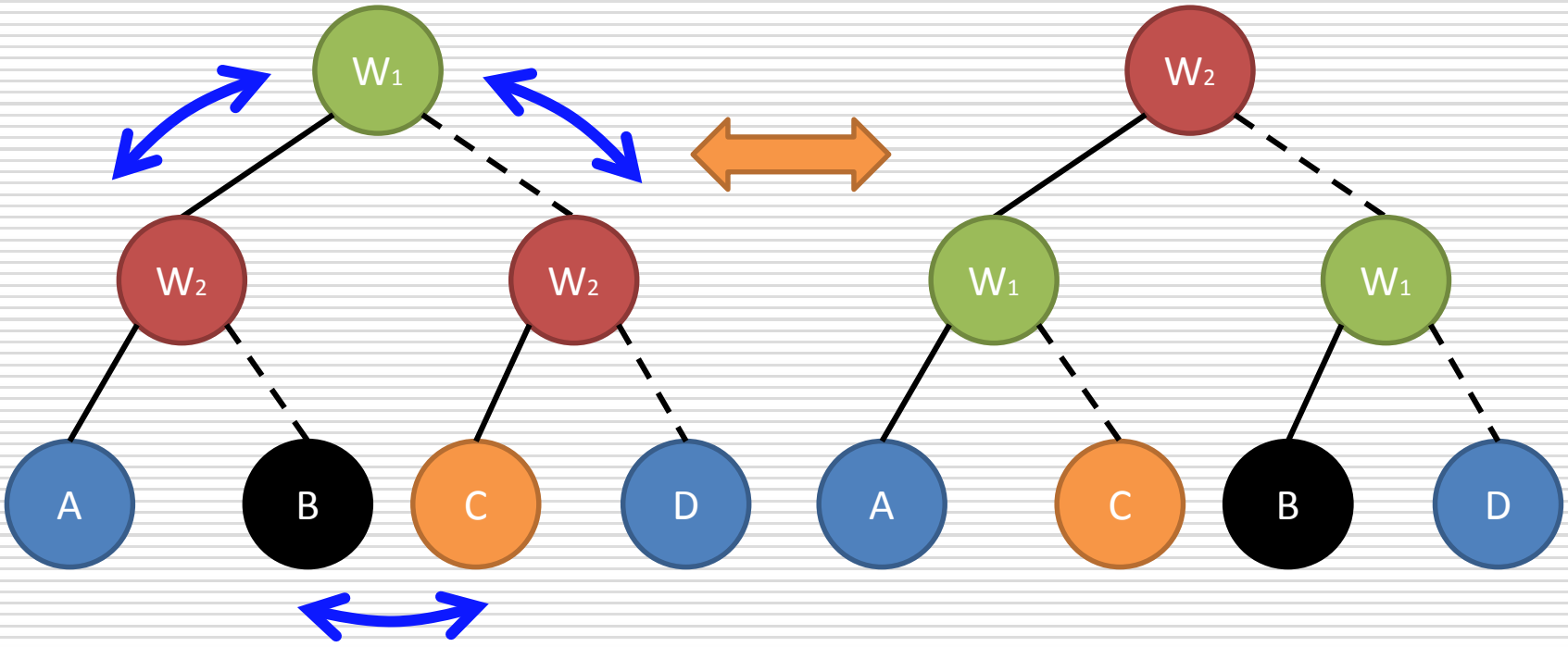


- Insertion position



Symbol Reordering

- Fundamental Case Consideration
- Traverse all GPDD node on the level W_1



Symbol Reordering

- Sift the incremental symbol in symbol table

Symbol Table	Symbol Table	Symbol Table	Symbol Table
X	X	X	X
S	A	A	A
A	S	B	B
B	B	S	C
…	…	…	…
N	N	N	S

Origin

Symbol Reordering

- Sift the incremental symbol in symbol table

Symbol Table
X
S
A
B
…
N

Origin

Symbol Table
X
A
…
S
…
N

Best Pos based on |GPDD|

Symbol Table
X
A
B
C
…
S

Symbol Reordering

- Sift the incremental symbol in symbol table

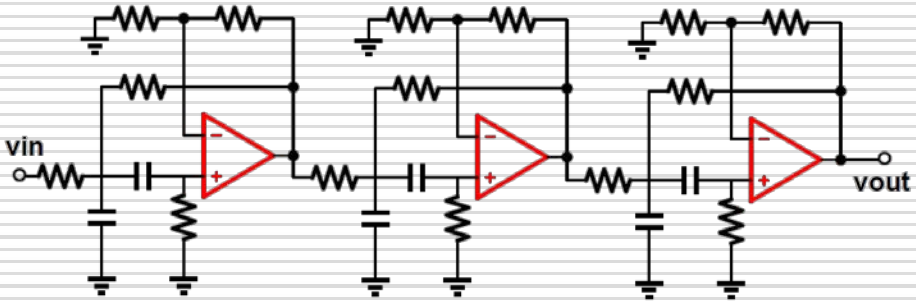
Symbol Table
X
S
A
B
…
N

Origin

Symbol Table
X
A
…
S
…
N

Final

Band-pass Filter with three Opamps



Test Case	|GPDD|	Time (ms)
One shot w. pre-order	160	31.00
Inc. w/o sifting	2,141	1,042.70
Inc. with sifting	326	1,334.30

Conclusion

- Proposed an Incremental GPDD algorithm to trace circuit topology change incrementally.
- Implemented a symbol reordering method to optimize an incrementally created GPDD.

Thanks!
Q & A!