SPICE Model of Polyswitch Device

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***Abstract*—Polymer Positive Temperature Coefficient thermistor (PPTC) as a polyswitch for circuit protection is not a standard circuit element for SPICE simulation, which hinders circuit performance evaluation and prediction. Physics-based model written in SPICE engine is of advantage in speed and accuracy, however, it is impractical for every device engineers to build a physical theory and rewrite a SPICE engine to simulate a new device. This report illustrates a novel circuit architecture with pre-existing SPICE elements for PPTC simulation. Three types of PPTCs, miniSMDC014F, miniSMDC050F, miniSMDC150F-24, offered by TE Connectivity, are verified for this method. The related data and netlist, including library usage, are provided.**

***Index Terms*—SPICE model, polyswitch, curve fitting, positive temperature coefficient thermistor (PTC).**

I. Introduction

Polyswitch devices are mainly designed for circuit protection. When the current flowing through the device or the voltage across it reaches dangerous region, the device resistance rises dramatically to protect the rest of circuit from damage. This kind of behaviour is also called trip. Since the thermal power induced by excess current or voltage can be regarded as the equivalence of the device temperature, the polyswitch devices are most implemented by thermistors.

There are two categories of thermistors: positive temperature coefficient thermistor (PTC) and negative one (NTC). The resistance of PTC grows as the temperature increases, while NTC acts the opposite. Three types of thermistors provided by *TE Connectivity*, miniSMDC014F, miniSMDC050F and miniSMDC150F-24, belong to PTC, and are fabricated by polymer material [1], therefore, they are also named as polymer PTC (PPTC).

Due to the lack of relevant SPICE model for PPTC devices, designers are unable predict the entire circuit behaviours with PPTCs by SPICE simulation before actual testing, which may result in extra cost for fabrication and testing. The conventional SPICE device model are implemented inside the simulation engine, which are usually physics-based. Although PPTC also has its corresponding physical model [2], developing such a device model requires source code of simulation engine and relevant knowledge about electronic design automation (EDA), which is unpractical for most device engineers. Another available choice is to build an equivalent circuit holding the same properties as PPTC. The authors of [3], [4] proposed to circuit structures with low and high resistance states for emulating abrupt switching behaviour of PPTC. The methods in [3], [4] are simple enough for understanding and construction, however, the proposed netlist can't adapt itself to different ambient temperature and fault current, limiting the simulation flexibility of the SPICE model.

This report demonstrates a novel circuit structure for PPTC SPICE model with switching and tripping behaviour, suitable for various ambient temperature and fault current. The article is organized as follows. Section II reviews some fundamental parameters and related definitions of PPTC, and also discusses the curve fitting procedure for parameter extraction. The entire circuit system for PPTC model is illustrated and analyzed in Section III. Several experimental examples are given in Section IV to validate the effectiveness of the SPICE model in OrCAD PSPICE. Section V concludes the paper.

II. Characteristic Parameter of PPTC

PPTC owns numerous key parameters determining its action, mainly in three aspects: resistance, current and time. This section gives the definition of various PPTC parameters, and points out what counts in SPICE modeling. The curve fitting methodology is also illustrated and fully discussed. The *curve fitting tool* (cftool) provided by MATLAB has been applied for fitting calculation.

A. Resistance

Many kinds of resistance definition can be found in [1]. Here are some of the definitions.

- R_i The initial resistance range of a population of devices as delivered to the customer.
- R_{min} The lower boundary of the initial resistance spec.
- R_{max} The upper boundary of the initial resistance spec.
- R_{1max} The maximum resistance that the device is expected to exhibit one hour after reflow and/or exposure to one trip event.

Actually, all of the resistance definitions above imply the underlying concept of fabrication variation. However, for a PPTC SPICE model, the variation doesn't facilitate to construct the basic circuit function. We just concern two simple values as required, the ordinary resistance when circuit behaves well and the abnormal resistance for circuit protection. The transition procedure from ordinary resistance to abnormal one is called trip as a PPTC term. In this report, the ordinary resistance is called *low-state resistance* R_L, since the resistance in this situation is normally small, and we also have *high-state resistance* R_H denoting the resistance for circuit protection, which is often very large.

Given the relationship between temperature and the ordinary resistance, R_L is easily determined by single variable, ambient temperature. Due to the rapid rise of resistance at some temperature shown in the given data, an arc tangent function with a linear calibration has been applied as follows.

$$\log_{10} R_L = \lambda \arctan\left[\alpha\left(T - T_{mid}\right)\right] + \kappa T + \beta \tag{1}$$

Apparantly, as long as λ, α and κ are all positive, the strictly increasing monotonicity of PPTC R-T curve can be easily proven, which ensure the correctness of PTC definition. The turning points T_{mid} of curve have been well captured, and the monotonicity has been assured in Fig. 13 in Appendix C. It is remarkable that normalization in data pre-processing has a significant impact affect on the fitting performance. For both resistance and temperature, the mean value is first cancelled, and then the standard deviation is divided. In addition, due to large span of the data, ranging from 0.1Ω to $10M\Omega$, therefore fitting procedure only takes resistance in log scale, even before normalization, which means that tiny mismatch in the curves shown in Fig. 13 may lead to huge gaps on the order of magnitude. If some physics-based equations of this kind of PPTC are provided, more accurate fitting results can be achieved hopefully. Shown in Line 54 of Netlist 1 in Appendix A is the realization of Eqn. 1 in SPICE netlist. Readers are encouraged to replace the equation for better performance.

When the trip action is taken, PPTC has a constant thermal power consumption P_D to limit the flowing current, thus high-state resistance can be determined as follows:

$$R_H = \frac{V^2}{P_D} \tag{2}$$

Here denoted by V is the voltage across the PPTC after trip. We use a linear model below to fit the relationship between power dissipation coefficient P_D and ambient temperature as shown in Fig. 12 in Appendix C.

$$P_D = k_{Pow} T + b_{Pow} \tag{3}$$

The expansive and time-consuming test for power dissipation coefficient P_D largely confines the amount of data, resulting in low order fitting model to prevent overfitting.

B. Current

There are two principle current concepts in PPTC parameters: hold current I_{Hold} and trip current I_{Trip}. Here are these two definitions.

- I_{Hold} The maximum current at which the device won't trip.
- I_{Trip} The minimum current at which the device will always trip.

Like the parameter definitions in Section II-A, these definition are related to variation, however, taking hold current I_{Hold} as the threshold current for PPTC to trip suits best for conservative consideration of simulation prediction of the device behaviour. Moreover, the hold current has a linear dependence on the ambient temperature.

$$I_{Hold} = k_{Cur} T + b_{Cur} \tag{4}$$

Therefore, a linear as shown in Eqn. 4 is applied for data fitting. The fitting results shown in Fig. 11 in Appendix C demonstrate the accuracy and usefulness of hold current.

C. Time

The trip doesn't take place immediately after the circuit fault happens, instead, there is a delay called *Time-to-Trip* TtT between PPTC trip action and appearance of the fault current. Time-to-Trip TtT enables the transition from low-state to high-state via heating the device to sufficient device temperature for trip. When the fault current is relatively large, the accumulation of the device heat will be accelerated, shortening Time-to-Trip TtT. On the other hand, if the ambient temperature is high, since the device itself is already hot enough, Time-to-Trip TtT will also shrinks a lot. Hence, Time-to-Trip TtT is related to fault current and ambient temperature. A 4th-order polynomial equation below has been applied for curve fitting.

$$\log_{10} TtT = \sum_{i=0}^{4} \sum_{j=0}^{4-i} p_{ij} T^i I^j \tag{5}$$

The fitting results are shown in Fig. 14 in Appendix C. Like what was illustrated in Section II-A, due to the extensive data range and a modicum of test data, the fitting performance is greatly constrained, and the number of feature is restricted, as well. Eqn. 5 is represented in Line 30 of Netlist 1 in Appendix A, which may be improved by advanced fitting model on the basis of physics or more data and better feature engineering.

It is worth noting that overflow or underflow in SPICE engine is likely to take place in Eqn. 5, therefore upper and lower bound are set to $1Ks$ and $10ns$, respectively.

Remark 1: Due to the data scarcity, all the data is utilized for data fitting, other than the traditional practice in machine learning problem with three types of data sets, training set, cross-validation set and test set.

III. Circuit Implementation

Unlike the traditional SPICE device model stamping into a modified nodal analysis (MNA) matrix, this PPTC SPICE model is implemented by a bunch of pre-existing circuit elements. The system architecture for PPTC is first considered, then each main parts is fully dissected for further analysis.

A. System Architecture

In Section II, we can see that the four most important parameters are the low-state resistance R_L, high-state resistance R_H, hold current I_{Hold} and Time-to-Trip TtT. The underlying operatring principle of PPTC, as shown in Fig. 1, is the transition from low-state resistance to high-state one, satisfying two conditions: (1) Flowing current is larger than I_Hold. (2) Fault time is longer than TtT.

According to the basic concept illustrated in Fig. 1, the corresponding circuit architecture can be constructed as shown

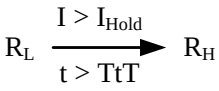


Fig. 1: PPTC architecture concept.

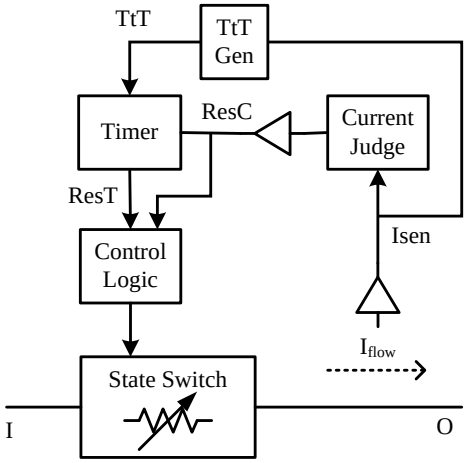


Fig. 2: PPTC system architecture.

in Fig. 2. Netlist 2 in Appendix A is the top block of the system.

State switch is the combination of low-state resistance and high-state resistance, which is main part of entire system. The *state switch* is set to low-state resistance under the default configuration. The current flowing through it are captured to judge whether it surpasses the hold current. $ResC$ will be 1 if the current outnumbers the threshold. In addition, *TtT generation* also requires the flowing current to create time threshold. If $ResC$ is 1, the *timer* starts to count, and when the timer's time exceeds TtT, $ResT$ is set to 1. If both $ResC$ and $ResT$ are 1, the *control logic* will tell *state switch* to alter the state to high-state.

Two buffers are inserted in the system loops via RC networks with $10ns$ time constant for simulation convergence. The upper buffer ensures the *timer* to obtain a stabalized TtT, and the other buffer is added for general loop convergence consideration. Without these buffers, SPICE simulation will end up with convergence problems.

B. State Switch

State switch shown in Fig. 2 is the principal circuit block in the whold system, which manifests the resistance feature of PPTC. Shown in Fig. 3 is the realization of state switch.

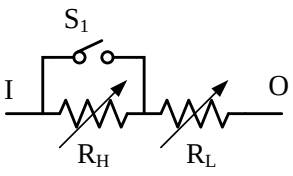


Fig. 3: State Switch.

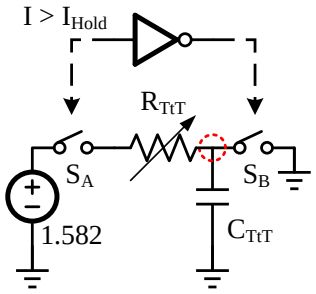


Fig. 4: Timer design.

The resistances of R_L and R_H are determined by Eqn. 1 and Eqn. 2, respectively. When S_1 is closed, the resistance of the state switch will be $R_L + R_{S_1} \approx R_L$, denoting low-state; when S_1 is open, the total resistance will be $R_L + R_H$. In most cases R_L is much smaller than R_H, therefore, $R_L + R_H$ is approximately equal to R_H, then the latter situation can be regarded as high-state. The state switch is described from Line 49 to 59 in Netlist 1 in Appendix A.

C. Timer Design

Shown in Fig. 4 is the circuit for timer, written from Line 13 to 26 in Netlist 1 in Appendix A. A simple low-pass RC circuit with several switches is applied for time counting. R_TtT is a variable resistor to adjust the time constant of R_{TtT} and C_{TtT} to the required TtT. Thanks to the time constant embedded in the impulse response, when the flowing current is larger than I_{Hold}, which means S_A is closed and S_B is open, the voltage in the red circle can be expressed by the equation below. The input voltage here approximates to $\left(1 - e^{-1}\right)^{-1}$.

$$V = V_{in}\left(1 - e^{-\frac{t}{R_{TtT}C_{TtT}}}\right) = V_{in}\left(1 - e^{-\frac{t}{TtT}}\right) \quad (6)$$

Therefore, if the voltage in the red circle outnumbers $1V$, the timer's time exceeds TtT, and $ResT$ in Fig. 2 is set to 1. When the current is smaller than I_{Hold}, S_B is closed, hence both ports of C_{TtT} are short to the ground, discharging all the charges storing in the capacitor, then the entire timer is reset. Moreover, since the closed switch still has some parasitic resistance, which will be added to R_{TtT}, the resistance of R_{TtT} is set to $TtT \times 1M\Omega$, and the capacitance of C_{TtT} is $1\mu F$. Furthermore, the off-resistance of the switch S_B is also required as large as possible to lessen the voltage across the switch.

D. Control Logic

The main purpose of the control logic is to alter the state of state switch via controlling the S_1 in Fig. 3. The results of current judgement ($ResC$) and timer ($ResT$) are sent to a *AND gate* to verify whether both current and time conditions are satisfied to make PPTC trip, then a SR latch is utilized to ensure the unidirection state transition as shown in Fig. 5. The related SPICE description can be found from Line 34 to 47 in the netlist in Appendix A.

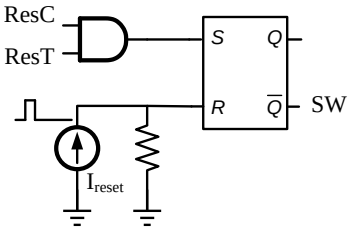


Fig. 5: Control logic for state switch.

TABLE I: Truth table of SR latch

S	R	Q	$\overline{Q}$
0	0	Keep	Keep
0	1	0	1
1	0	1	0
1	1	Undefined	Undefined

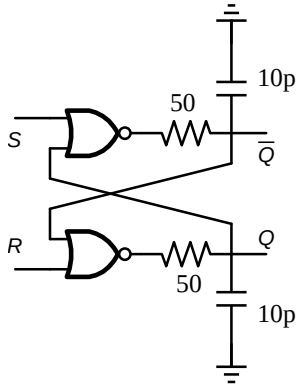


Fig. 6: SR latch.

SR latch is a typical digital sequential gate, its *truth table* shown in Table I reveals its working mechanism. An initial pulse resets the SR latch to 0. Once the *AND gate* output is 1, the SR latch is kept at 1, thus, PPTC won't trip back to low-state resistance unless the simulation is stopped. Shown in Fig. 6 is the circuit implementation of SR latch with two RC networks for simluation convergence consideration.

Actually, there is a third condition for the *AND gate* here. When the ambient temperature is larger than a certain point, the PPTC can be regarded as the high-state resistance, so there is no need for it to go through another trip action. In this work, when the temperature is higher than $126°C$, the S_1 as shown in Fig. 3 will always be closed.

IV. Experimental Results

The SPICE model for PPTC is experimented by OrCAD PSPICE 16.6 in a personal computer. Two types of simluation are taken to validate the effectiveness of the PPTC model in time domain and temperature domain, using miniSMDC014F data.

The first test is taken in temperature domain to present the resistance variance of PPTC under various ambient temperature. Shown in Fig. 7 is the test circuitry. By sweeping temperature, different voltages V_R across the PPTC should be observed.

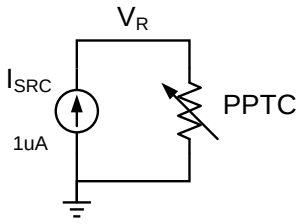


Fig. 7: Test circuitry for temperature domain.

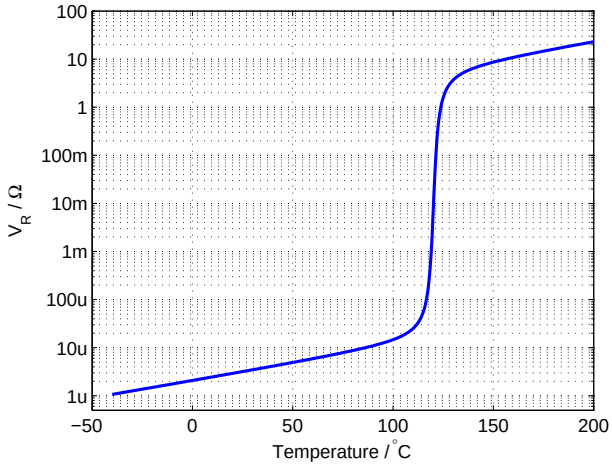


Fig. 8: Temperature domain test result.

The value of the current source is set $1\mu A$ to avoid trip in advance. Shown in Fig. 8 is the result of V_R in PSPICE.

The curve shape is just similar to the one as shown in Fig. 13. The voltage across the PPTC is drawn here, therefore all data should be divide by 1μ to get the actual resistance.

Another test is experimented in time domain to demonstate the trip action in PPTC. Shown in Fig. 9 is the related test circuitry.

The load resistance R_L is set to 50Ω under room temperature $27°C$, and the voltage source V_{Pulse} provides a pulse from $5V$ to $100V$ at $1\mu s$ as working voltage and fault voltage, respectively. The result of output voltage V_{Out} is given in Fig. 10.

The blue line denotes the input pulse, and the red line gives the output voltage. When the fault happened, the PPTC first works as the normal low-state resistor, after the corresponding Time-to-Trip, the output voltage decreases suddenly, acting as the high-state resistor then, which verified the effectiveness of

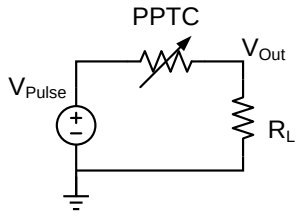


Fig. 9: Test circuitry for time domain.

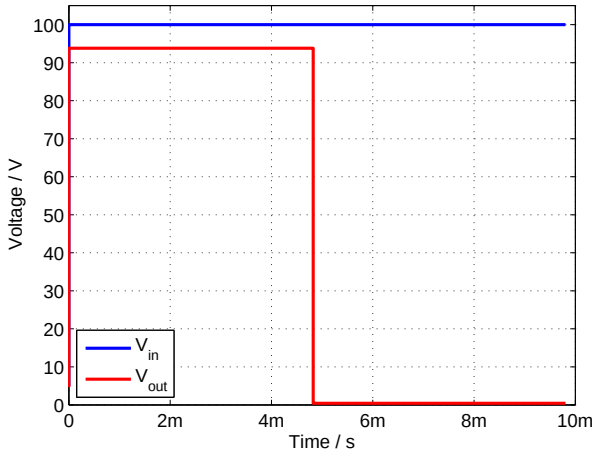


Fig. 10: Time domain test result.

the model.

Although the polyswitch is a resettable device, after tripping, the PPTC remains at high-state, unless the PPTC is disconnected from the circuit. The polyswitch always works fine even if it has already tripped, however, due to the resistance equation for high-state, in some special case, the simulation will fail. For example, if the PPTC resistance is determined by Eqn. 2 and all other parasitic are neglected, then the output voltage can be given as follows.

$$V_{Out} = \frac{V_{in} - \sqrt{V_{in}^2 - 4R_L P_D}}{2} \tag{7}$$

Therefore, after PPTC trips, when the input voltage is too low, simulation will result in error. This kind of situation is ignored in this work.

V. Conclusion

The characteristic parameters are reviewed, and the relevant circuit implementation is illustrated in this report. Several experimental results are given to demonstrate the usefulness and validity of the PPTC model for SPICE simulation. A number of key points attempt to relieve the convergence problem, which enlarges the scope of model appliation. This work provides a general model for PPTC SPICE simulation, and for a particular PPTC type, a new PPTC model is easily regenerated when offering related equations and parameters.

Appendix

A. Model Netlist

A PPTC library mainly contains two files, *pptc.lib* and a file named as a particular type of PPTC, such as: *miniSMDC014F.lib*. For the sake of usage convenience in PSPICE and clean code, the *pptc.lib* is seperated as a single file and serves as a general circuit template providing the fundamental building blocks for PPTC family shown in Netlist 1.

Netlist 1: PPTC.lib

```
1  *PPTC lib
2
3  *Switch model
4  .model S_model VSWITCH(RON=1m ROFF=1G
       VON=1 VOFF=0)
5
6  * Current Judgement
7  .subckt JCur Vcur out PARAMs: ithb=1
       ithk=0
8  Ejudge in 0 VALUE {IF((V(Vcur,0) >=
       ithk*temp+ithb),1.581977, 0)}
9  Rd in out 1
10 Cd out 0 10n
11 .ends
12
13 * Time to trip Judgement
14 .subckt JTtT set vTtT out
15 * Time Counting
16 Vin in 0 1.581977
17 Sset tmp in set 0 S_model
18 G1 tmp JPoint VALUE {1u*V(tmp, JPoint)
       /V(vTtT,0)}
19 C1 0 JPoint  1u
20 * Time reset (discharge C1)
21 Sreset JPoint 0 reset 0 S_model
22 * inverter
23 Einv reset 0 VALUE {IF((V(set) >= 0.5)
       ,0, 1)}
24 * judgement
25 Ejudge out 0 VALUE {IF((V(JPoint,0) >=
        1),1, 0)}
26 .ends
27
28 * TtT Generation
29 .subckt TG Isen TtT PARAMs: p00=0 p10
       =0 p01=0 p20=0 p11=0 p02=0 p30=0
       p21=0 p12=0 p03=0 p40=0 p31=0 p22=0
        p13=0 p04=0
30 Gtg 0 TtT VALUE {pwr(10,min(max(p00+(
       p10+(p20+(p30+p40*temp)*temp)*temp)
       *temp+(p01+(p11+(p21+p31*temp)*temp
       )*temp)*V(Isen)+(p02+(p12+p22*temp)
       *temp)*V(Isen)*V(Isen)+(p03+p13*
       temp)*V(Isen)*V(Isen)*V(Isen)+p04*V
       (Isen)*V(Isen)*V(Isen)*V(Isen),-8)
       ,3))}
31 Rtg TtT 0 1
32 .ends
33
34 * Switch State Control
35 .subckt SSC resC resT Q_
36 * Reset Signal
37 VR R 0 PWL 0 1 0.9n 1 1n 0
38 * SR Latch
```

```
Esr1 Qt 0 VALUE {IF(((V(R) < 0.5) & (V(Q_) < 0.5)), 1.581977,  0)}
RD1 Qt Q 50
CD1 Q 0 10p
Esr2 Qt_ 0 VALUE {IF(((V(Q) < 0.5) & (V(S) < 0.5)), 1.581977,  0)}
RD2 Qt_ Q_ 50
CD2 Q_ 0 10p
* And Gate
Eand S 0 VALUE {IF(((V(resC) >= 0.5) & (V(resT) >= 0.5) & (temp <= 126)), 1, 0)}
.ends

* Main Part
.subckt MP I O LC Isen PARAMs: brl=0 krl=0 crl=0 arl=0 tmid=0 pdk=0 pdb=1
Vsen I 1 0
SL 1 2 LC 0 S_model
GH 1 2 VALUE {V(1,2)/(V(I,O)*V(I,O)/max((pdk*temp+pdb),1e-9))}
GL 2 O VALUE {V(2,O)/pwr(10,(krl*temp+brl+crl*atan(arl*(temp-tmid))))}
* Current Sensing
Rsen Isen 0 1
Csen Isen 0 10n
Gsen 0 Isen Value {abs(I(Vsen))}
.ends
```

The other file gives the specified parameters and integrates all the blocks together for a particular PPTC type as follows.

Netlist 2: miniSMDC014F.lib

```
*miniSMDC014F PPTC library

.include 'pptc.lib'

.subckt miniSMDC014F I O
* Main Framework
Xmp I O LC Isen MP PARAMs: brl=3.1407 krl=7.0713e-3 crl=1.8143 arl=0.532 tmid=120.186 pdk=-0.008497 pdb=1.105
XTG Isen TtT TG PARAMs: p00=3.041 p10=-0.02291 p01=-4.108 p20=-0.0001655 p11=0.006464 p02=0.8491 p30=4.918e-06 p21=0.0001054 p12=-0.000808 p03=-0.04981 p40=-3.623e-08 p31=-8.776e-07 p22=-7.133e-06 p13=4.238e-05 p04=0
XJC Isen resC JCur PARAMs: ithb=0.1679 ithk=-0.00129
XJT resC TtT resT JTtT
XSSC resC resT LC SSC
.ends
```

The circuit netlist of miniSMDC014F is taken as an example in Netlist 2. It can be seen that each building block described in Section III is implemented by a sub-circuit, including *JCur*, *JTtT*, *TG*, *SSC* and *MP*, and the whole system is packed in the top sub-circuit named as the PPTC type (Here is *miniSMDC014F*.) as shown in Netlist 2 where the corresponding parameters are also given.

All the logic circuits here are implemented by voltage-controlled voltage sources (VCVSs), denoted by *E* in the netlist, with special assignment. Moreover, voltage-controlled current sources (VCCSs), denoted by *G*, are used to substitute the variable resistors in the circuit. Since VCCS follows the equation $I_{out} = GV_{in}$, Ohm's law is achieved when we assign G with transconductance of the resistor $1/R$.

B. Library Usage

The usage of the SPICE PPTC model in OrCAD 16.6 Lite is described here. Since the given model is written in SPICE, the library compatible with PSPICE (*.olb* file) should be produced first. In addition, related symbols should be associated to the generated library. Here is the detailed procedure for usage (miniSMDC014F.lib is taken as an example):

Step 1 Open *PSPICE Model Editor*.
Step 2 Click *Open* in *File* menu to open the library for a specified PPTC *miniSMDC014F.lib*.
Step 3 Click *Export to Capture Part Library* in *File* menu to generate *.olb* file.
Step 4 Click *Model Import Wizard [Capture]* in *File* menu to associate symbols with the devices.
Step 5 Open *OrCAD Capture CIS*.
Step 6 Add the generated *.olb* file to the library in *Project File Browser*.
Step 7 Add both library files *pptc.lib* and *miniSMDC014F.lib* to the *Simulation Setting Dialog*.
Step 8 Now the PPTC model in PSPICE can be applied in *Part Manager*.

Given the original SPICE library, customization of the symbols in PSPICE is easy to accomplished, and engineers are also encouraged to observe and improve the implementation of the device model.

C. Data Results

The fitting parameters of the three PPTC types are given in this section and the relevant curve fitting figures will be depicted, as well.

1) Hold Current vs Temperature:

Linear model is applied to fit the relationship between ambient temperature and hold current I_{Hold}. Shown in Table II are the corresponding slopes and intercepts of the three PPTC types.

TABLE II: Parameters of hold current vs temperature

PPTC Type	Slope k_{Cur} (I/T)	Intercept b_{Cur} (I)
miniSMDC014F	-0.00129	0.168
miniSMDC050F	-0.00339	0.557
miniSMDC150F-24	-0.01197	1.721

In addition, the fitting curve results of the three PPTC types are shown in Fig. 11.

2) Power Dissipation vs Temperature:

Linear model is applied to fit the relationship between ambient temperature and power dissipation coefficient P_D determining the high-state resistor. Shown in Table III are the corresponding slopes and intercepts of the three PPTC types.

TABLE III: Parameters of power dissipation vs temperature

PPTC Type	Slope k_{Pow} (W/T)	Intercept b_{Pow} (W)
miniSMDC014F	-0.00850	1.105
miniSMDC050F	-0.00795	1.063
miniSMDC150F-24	-0.01177	1.461

In addition, the fitting curve results of the three PPTC types are shown in Fig. 12.

3) Low-state Resistance vs Temperature:

An arc tangent model with linear part has been applied to fit the relationship between ambient temperature and low-state resistance R_L, the detailed equation of the Gaussian model can be found in Section II. Table IV gives the corresponding parameters of the three PPTC types.

TABLE IV: Parameters of low-state resistance vs temperature

Parameter	miniSMDC014F	miniSMDC050F	miniSMDC150F-24
T_{mid}	120.186	123.889	126.081
κ	7.0713e-3	4.7e-3	3.842e-3
β	3.1407	2.8898	0.82754
α	0.532	0.597	0.524
λ	1.8143	2.04114	1.3223

In addition, the fitting curve results of the three PPTC types are shown in Fig. 13.

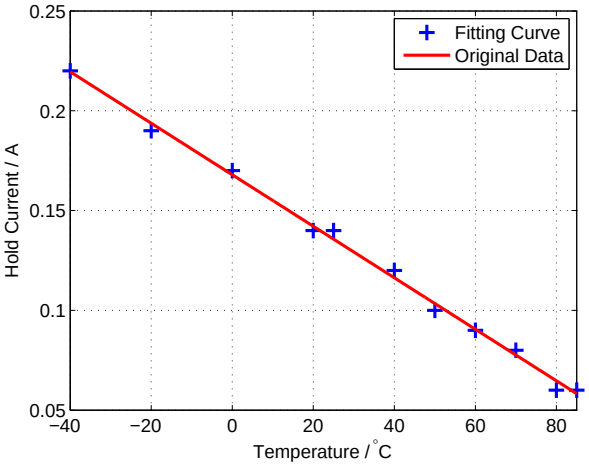
4) Time-to-Trip vs Fault Current & Temperature:

A 4-order polynomial model has been applied to fit the relationship between ambient temperature, fault current and time-to-trip TtT, the detailed equation of the polynomial model can be found in Section II. Table V gives the corresponding parameters of the three PPTC types.

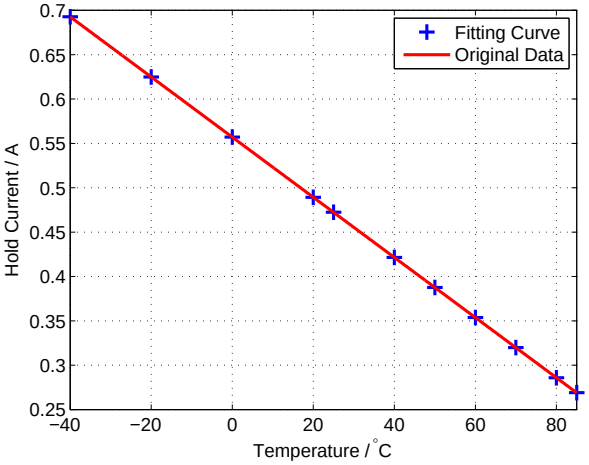
TABLE V: Parameters of Time-to-Trip vs fault current & temperature

Parameter	miniSMDC014F	miniSMDC050F	miniSMDC150F-24
p_{00}	3.041	3.458	2.688
p_{10}	-0.02291	-0.05439	0.01381
p_{01}	-4.108	-1.538	-0.5366
p_{20}	-0.0001655	9.813e-05	-0.0002564
p_{11}	0.006464	0.002681	-0.004829
p_{02}	0.8491	0.1375	0.02766
p_{30}	4.918e-06	2.057e-05	-3.709e-06
p_{21}	0.0001054	2.532e-05	2.138e-05
p_{12}	-0.000808	-0.000128	0.0004454
p_{03}	-0.04981	-0.003784	-0.0005195
p_{40}	-3.623e-08	-2.101e-07	4.594e-08
p_{31}	-8.776e-07	-1.442e-07	1.157e-08
p_{22}	-7.133e-06	-1.08e-06	-9.133e-07
p_{13}	4.238e-05	2.18e-06	-1.168e-05
p_{04}	0	0	0

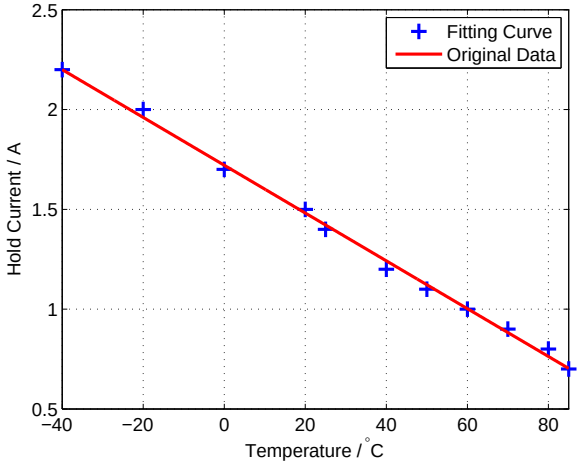
In addition, the fitting curve results of the three PPTC types are shown in Fig. 14.



(a) miniSMDC014F

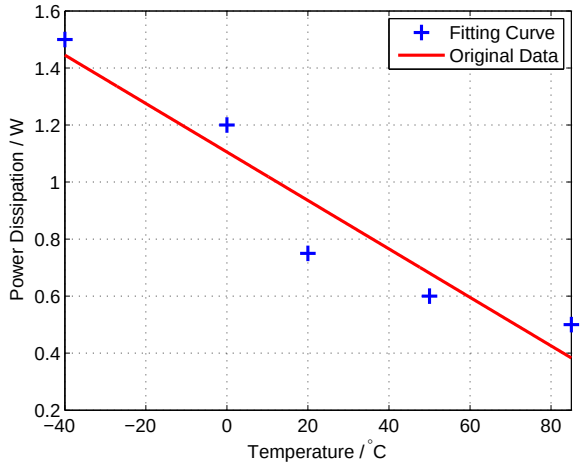


(b) miniSMDC050F

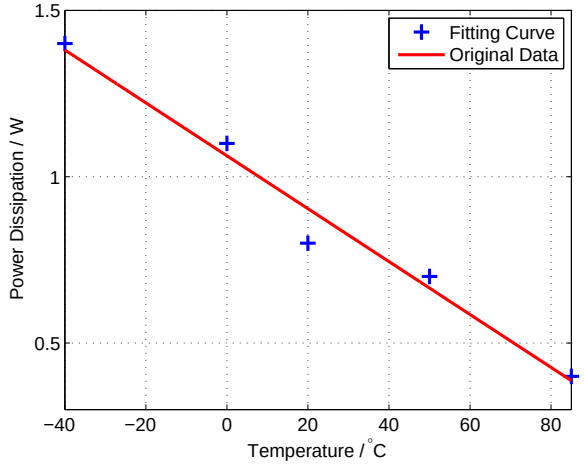


(c) miniSMDC150F-24

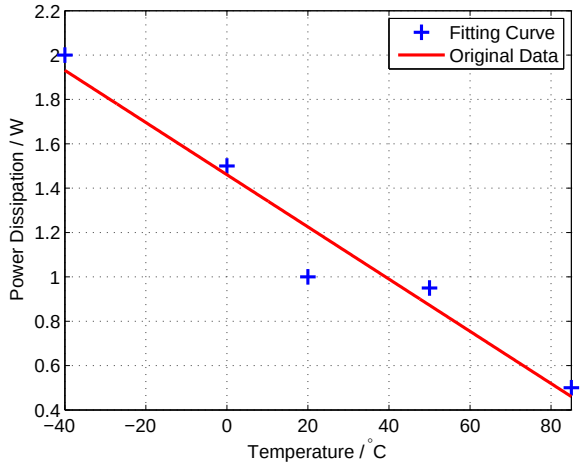
Fig. 11: Hold current vs temperature.



(a) miniSMDC014F

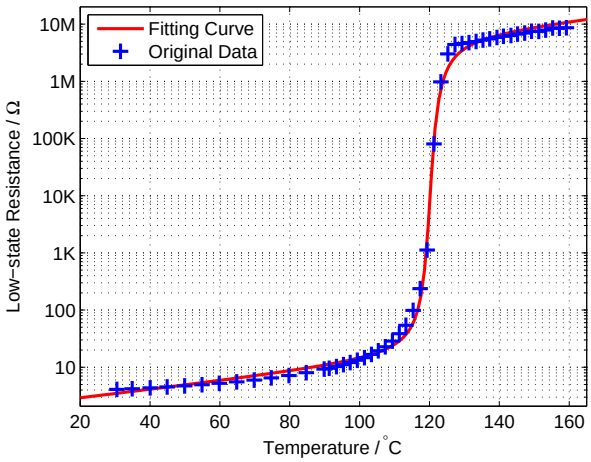


(b) miniSMDC050F

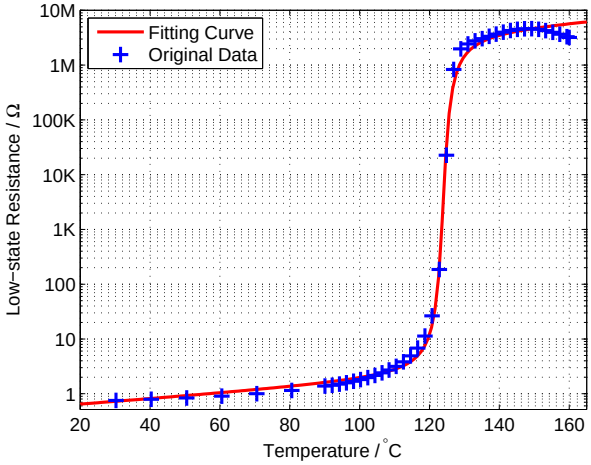


(c) miniSMDC150F-24

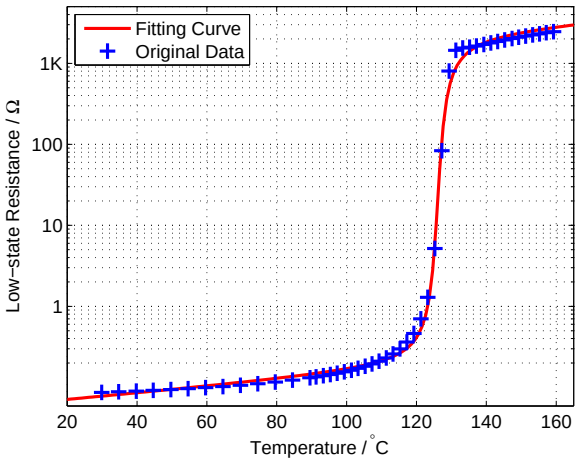
Fig. 12: Power dissipation vs temperature.



(a) miniSMDC014F

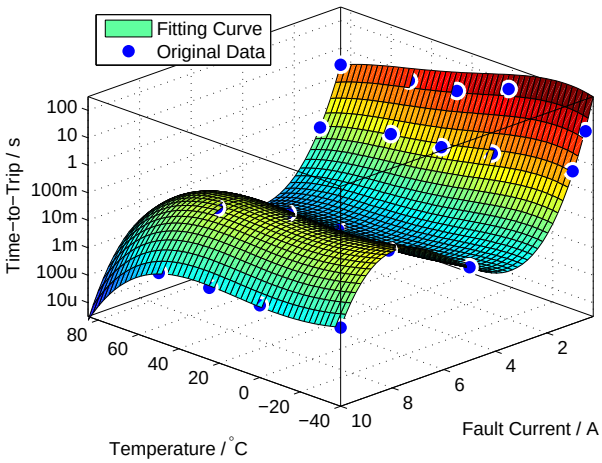


(b) miniSMDC050F

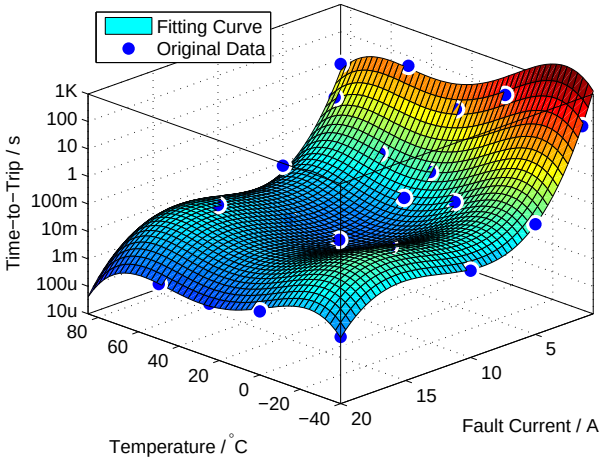


(c) miniSMDC150F-24

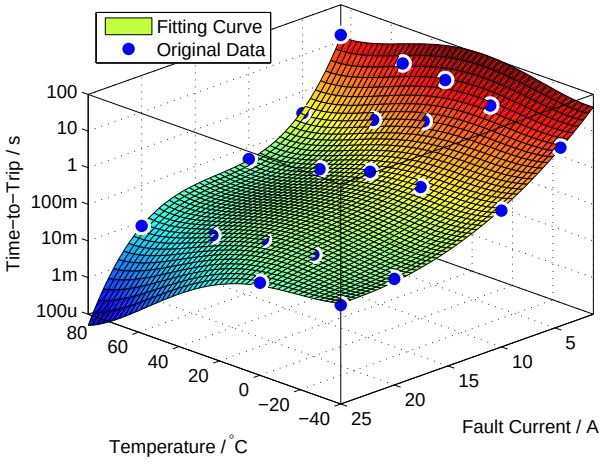
Fig. 13: Low-state resistance vs temperature.



(a) miniSMDC014F



(b) miniSMDC050F



(c) miniSMDC150F-24

Fig. 14: Time-to-Trip vs fault current & temperature.

REFERENCES

[1] TE Circuit Protection, *Circuit Protection Products Catalog 2013-2014*, TE Connectivity, Menlo Park, CA 94025, USA, 2013.

[2] M. A. Zubair and C. Leach, "Modeling the resistance-temperature characteristic of a positive temperature coefficient thermistor, using experimentally determined permittivity data," *Applied Physics Letters*, vol. 91, no. 8, p. 082105, 2007.

[3] I.-C. Tesu, "Spice simulation of thermistors and thermistor circuits," in *Proc. Mediterranean Electrotechnical Conference*, vol. 1, May 1991, pp. 79–82.

[4] C. Sheehan, "Spice model of mf-rm005 at 23c," https://www.bourns.com/data/global/engineering/MF-RM/MF-RM005-Tamb23C-SPICE.txt, June 2013.